CHAPTER 8

ANALOG & DIGITAL ELECTRONICS

YEAR 2012 **ONE MARK**

MCQ 8.1 In the sum of products function $f(X, Y, Z) = \sum(2,3,4,5)$, the prime implicants are

(A) $\overline{X}Y$, $X\overline{Y}$

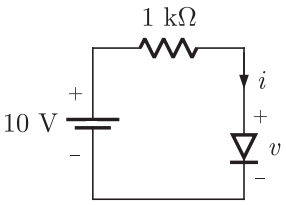
(B) $\overline{X}Y$, $X\,\overline{Y}\,\overline{Z}$, $X\overline{Y}Z$

(C) $\overline{X}Y\overline{Z}$, $\overline{X}YZ$, $X\overline{Y}$

(D) $\overline{X}Y\overline{Z}$, $\overline{X}YZ$, $X\overline{Y}\,\overline{Z}$, $X\overline{Y}Z$

MCQ 8.2 The i-v characteristics of the diode in the circuit given below are

$$i = \begin{cases} \dfrac{v - 0.7}{500}\ \text{A}, & v \geq 0.7\ \text{V} \\ 0\ \text{A} & v < 0.7\ \text{V} \end{cases}$$



The current in the circuit is

(A) 10 mA

(B) 9.3 mA

(C) 6.67 mA

(D) 6.2 mA

MCQ 8.3 The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

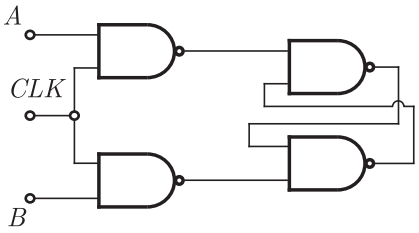
(A) 4

(B) 6

(C) 8

(D) 10

MCQ 8.4 Consider the given circuit



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In this circuit, the race around

(A) does not occur

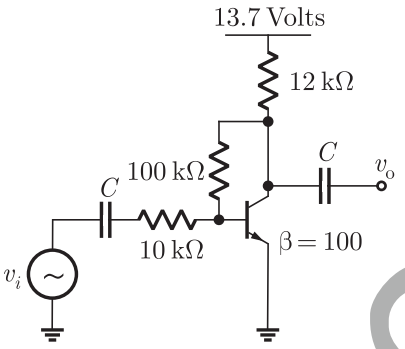
(B) occur when $CLK = 0$

(C) occur when $CLK = 1$ and $A = B = 1$

(D) occur when $CLK = 1$ and $A = B = 0$

YEAR 2012 TWO MARKS

MCQ 8.5 The voltage gain A_v of the circuit shown below is



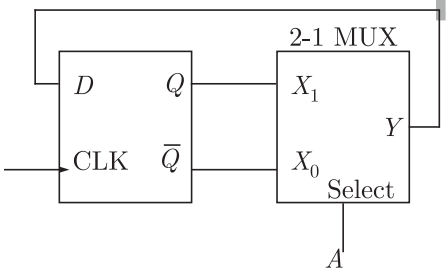
(A) $|A_v| \approx 200$

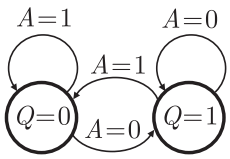
(B) $|A_v| \approx 100$

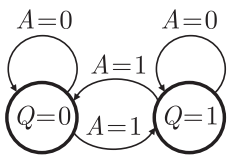
(C) $|A_v| \approx 20$

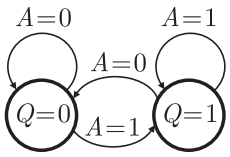
(D) $|A_v| \approx 10$

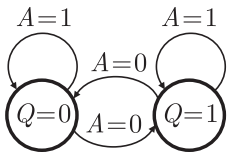
MCQ 8.6 The state transition diagram for the logic circuit shown is



(A)


(B)


(C)


(B)


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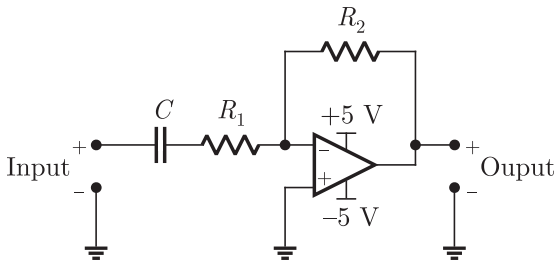
MCQ 8.7 The circuit shown is a



(A) low pass filter with $f_{3dB} = \dfrac{1}{(R_1 + R_2)\,C}$ rad/s

(B) high pass filter with $f_{3dB} = \dfrac{1}{R_1 C}$ rad/s

(C) low pass filter with $f_{3dB} = \dfrac{1}{R_1 C}$ rad/s

(D) high pass filter with $f_{3dB} = \dfrac{1}{(R_1 + R_2)\,C}$ rad/s

YEAR 2011 ONE MARK

MCQ 8.8 A low-pass filter with a cut-off frequency of 30 Hz is cascaded with a high pass filter with a cut-off frequency of 20 Hz. The resultant system of filters will function as

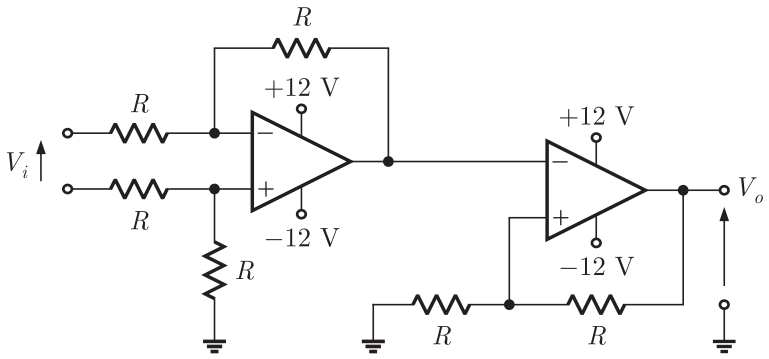
(A) an all – pass filter

(B) an all – stop filter

(C) an band stop (band-reject) filter

(D) a band – pass filter

MCQ 8.9



The CORRECT transfer characteristic is

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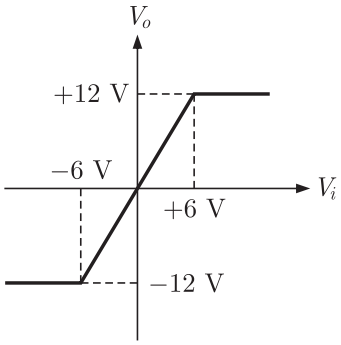
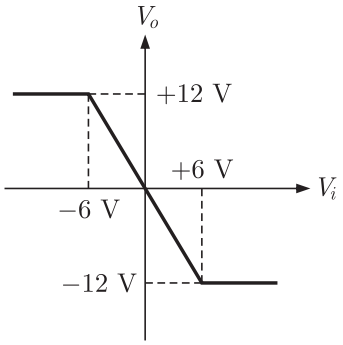
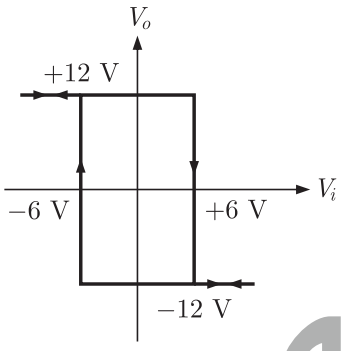
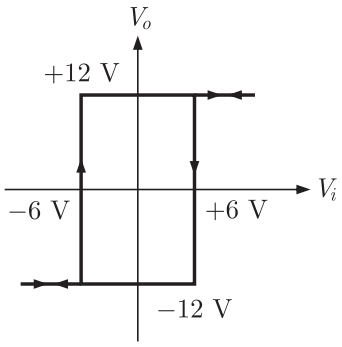
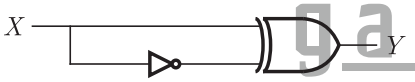
(A)


(B)


(C)


(D)


MCQ 8.10 The output Y of the logic circuit given below is



(A) 1
(B) 0
(C) X
(D) $\overline{X}$

YEAR 2011 **TWO MARKS**

MCQ 8.11 A portion of the main program to call a subroutine SUB in an 8085 environment is given below.

⋮
LXI D, DISP
LP : CALL SUB
LP+3
⋮

It is desired that control be returned to LP+DISP+3 when the RET instruction is executed in the subroutine. The set of instructions that precede the RET instruction in the subroutine are

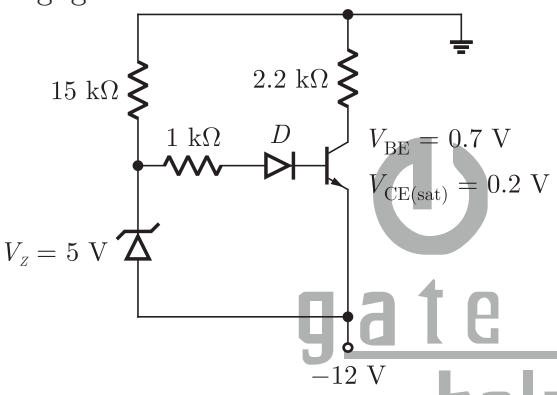
(A)
```
POP  D
DAD  H
PUSH D
```

(B)
```
POP  H
DAD  D
INX  H
INX  H
INX  H
PUSH H
```

(C)
```
POP  H
DAD  D
PUSH H
```

(D)
```
XTHL
INX  D
INX  D
INX  D
XTHL
```

MCQ 8.12 The transistor used in the circuit shown below has a β of 30 and I_{CBO} is negligible

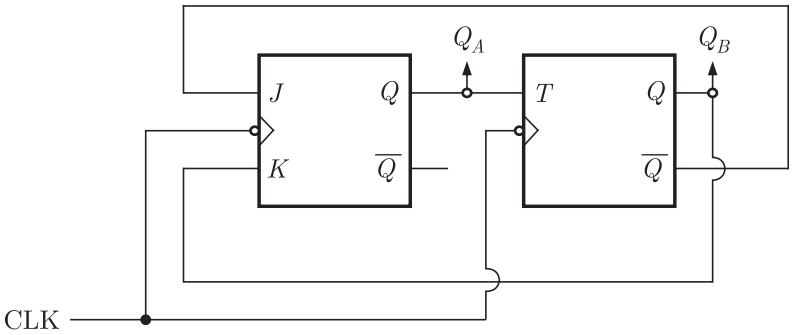


If the forward voltage drop of diode is 0.7 V, then the current through collector will be

(A) 168 mA (B) 108 mA

(C) 20.54 mA (D) 5.36 mA

MCQ 8.13 A two bit counter circuit is shown below

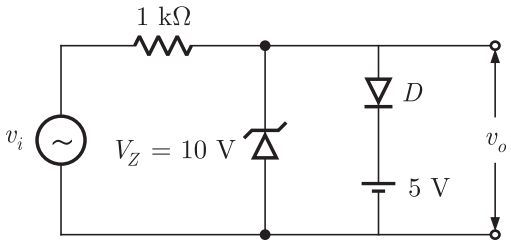


It the state $Q_A Q_B$ of the counter at the clock time t_n is '10' then the state $Q_A Q_B$ of the counter at $t_n + 3$ (after three clock cycles) will be

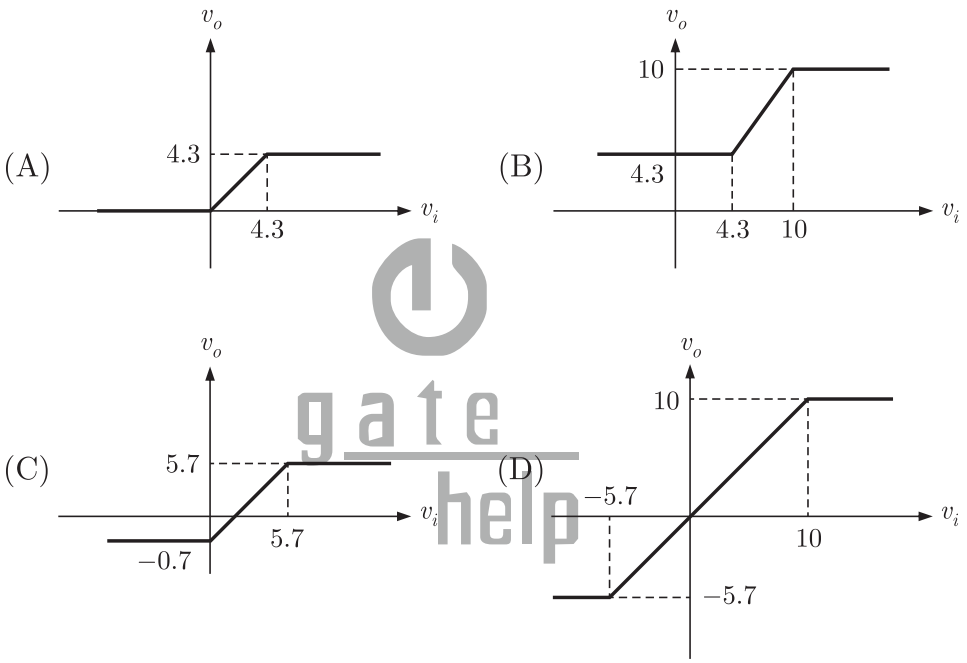
(A) 00 (B) 01

(C) 10 (D) 11

MCQ 8.14 A clipper circuit is shown below.

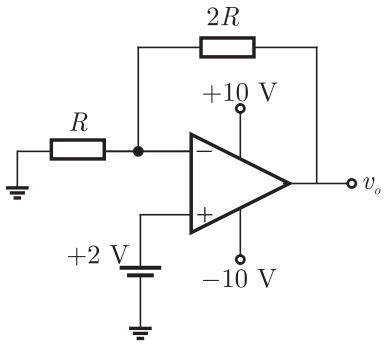


Assuming forward voltage drops of the diodes to be 0.7 V, the input-output transfer characteristics of the circuit is



YEAR 2010 **ONE MARK**

MCQ 8.15 Given that the op-amp is ideal, the output voltage v_o is



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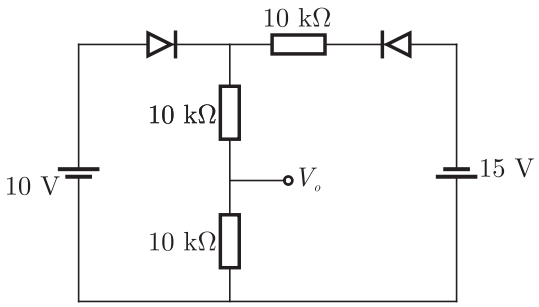
(A) 4 V (B) 6 V
(C) 7.5 V (D) 12.12 V

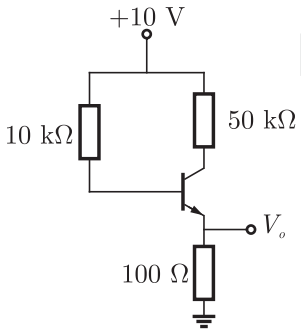
MCQ 8.16 Assuming that the diodes in the given circuit are ideal, the voltage V_0 is



(A) 4 V (B) 5 V
(C) 7.5 V (D) 12.12 V

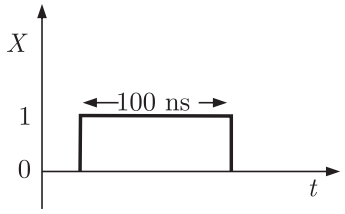
YEAR 2010 **TWO MARKS**

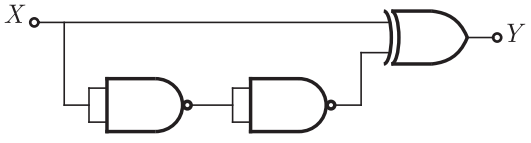
MCQ 8.17 The transistor circuit shown uses a silicon transistor with $V_{BE} = 0.7, I_C \approx I_E$ and a dc current gain of 100. The value of V_0 is



(A) 4.65 V (B) 5 V
(C) 6.3 V (D) 7.23 V

MCQ 8.18 The TTL circuit shown in the figure is fed with the waveform X (also shown). All gates have equal propagation delay of 10 ns. The output Y of the circuit is





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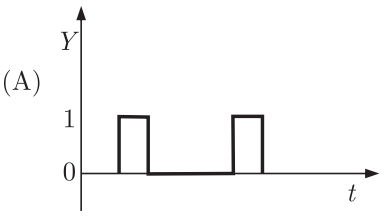
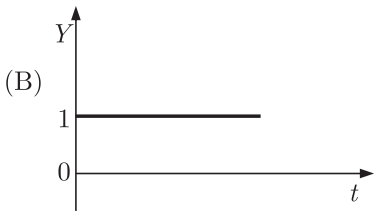
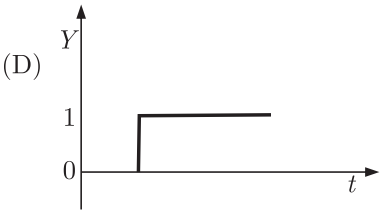
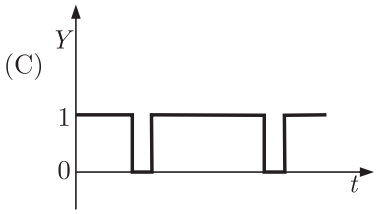
(A)


(B)


(D)


(C)


MCQ 8.19 When a "CALL Addr" instruction is executed, the CPU carries out the following sequential operations internally :

Note: (R) means content of register R
((R)) means content of memory location pointed to by R.
PC means Program Counter
SP means Stack Pointer

(A) (SP) incremented
(PC)←Addr
((SP))←(PC)

(B) (PC)←Addr
((SP))←(PC)
(SP) incremented

(C) (PC)←Addr
(SP) incremented
((SP))←(PC)

(D) ((SP))←(PC)
(SP) incremented
(PC)←Addr

Statement For Linked Answer Questions: 6 & 7

The following Karnaugh map represents a function F.

F : X \ YZ	00	01	11	10
0	1	1	1	0
1	0	0	1	0

MCQ 8.20 A minimized form of the function F is

(A) $F = \overline{X}\,Y + YZ$

(B) $F = \overline{X}\,\overline{Y} + YZ$

(C) $F = \overline{X}\,\overline{Y} + Y\,\overline{Z}$

(D) $F = \overline{X}\,\overline{Y} + \overline{Y}\,Z$

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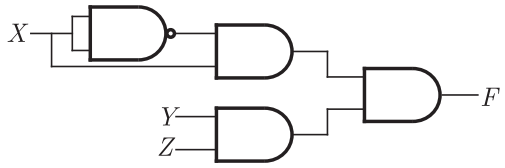
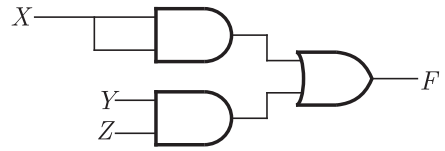
MCQ 8.21 Which of the following circuits is a realization of the above function F ?

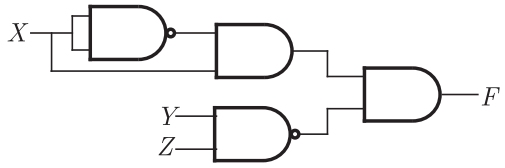
(A)



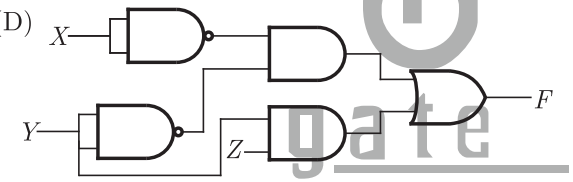
(B)



(C)

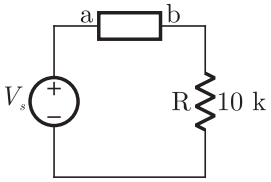


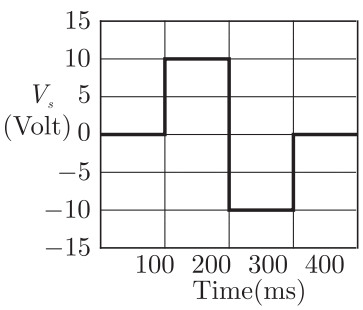
(D)

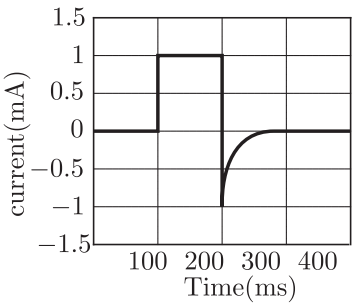


YEAR 2009 **ONE MARK**

MCQ 8.22 The following circuit has a source voltage V_S as shown in the graph. The current through the circuit is also shown.







The element connected between a and b could be

(A)

(B)

(C)

(D)

MCQ 8.23 The increasing order of speed of data access for the following device is

(I) Cache Memory

(II) CD-ROM

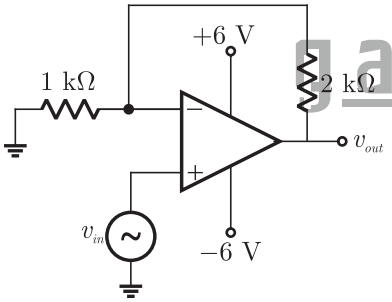
(III) Dynamic RAM

(IV) Processor Registers

(V) Magnetic Tape

(A) (V), (II), (III), (IV), (I)
(B) (V), (II), (III), (I), (IV)
(C) (II), (I), (III), (IV), (V)
(D) (V), (II), (I), (III), (IV)

MCQ 8.24 The nature of feedback in the op-amp circuit shown is



(A) Current-Current feedback
(B) Voltage-Voltage feedback
(C) Current-Voltage feedback
(D) Voltage-Current feedback

MCQ 8.25 The complete set of only those Logic Gates designated as Universal Gates is

(A) NOT, OR and AND Gates

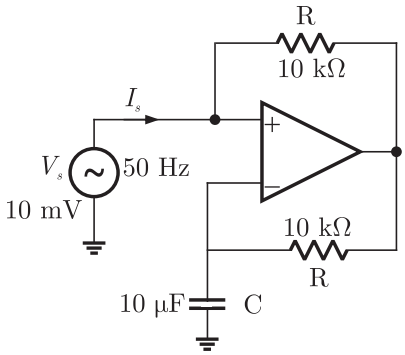
(B) XNOR, NOR and NAND Gates

(C) NOR and NAND Gates

(D) XOR, NOR and NAND Gates

YEAR 2009 TWO MARKS

MCQ 8.26 The following circuit has $R = 10\,\text{k}\Omega, C = 10\,\mu\text{F}$. The input voltage is a sinusoidal at 50 Hz with an rms value of 10 V. Under ideal conditions, the current I_s from the source is



(A) 10π mA leading by 90°
(B) 20π mA leading by 90°
(C) 10π mA leading by 90°
(D) 10π mA lagging by 90°

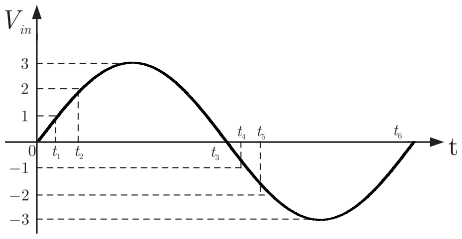
MCQ 8.27 Transformer and emitter follower can both be used for impedance matching at the output of an audio amplifier. The basic relationship between the input power P_{in} and output power P_{out} in both the cases is
(A) $P_{in} = P_{out}$ for both transformer and emitter follower
(B) $P_{in} > P_{out}$ for both transformer and emitter follower
(C) $P_{in} < P_{out}$ for transformer and $P_{in} = P_{out}$ for emitter follower
(D) $P_{in} = P_{out}$ for transformer and $P_{in} < P_{out}$ for emitter follower

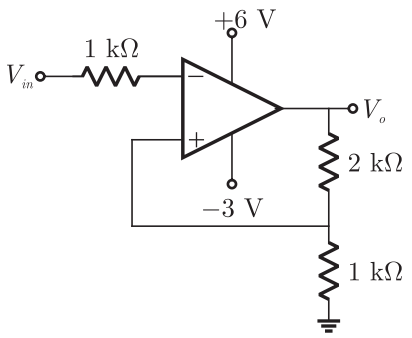
MCQ 8.28 In an 8085 microprocessor, the contents of the Accumulator, after the following instructions are executed will become

```
XRA  A
MVI  B, F0 H
SUB  B
```

(A) 01 H
(B) 0F H
(C) F0 H
(D) 10 H

MCQ 8.29 An ideal op-amp circuit and its input wave form as shown in the figures. The output waveform of this circuit will be





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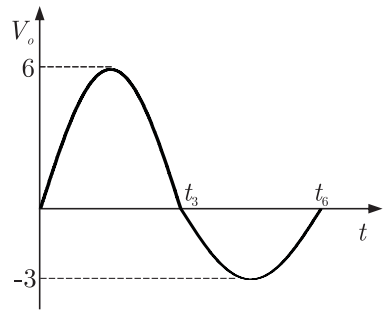
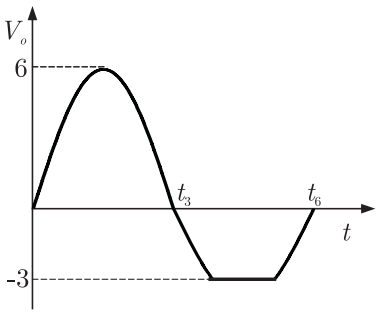
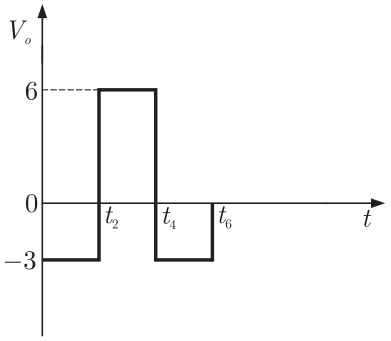
(A)



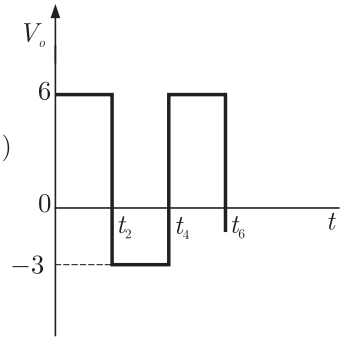
(B)



(C)



(D)

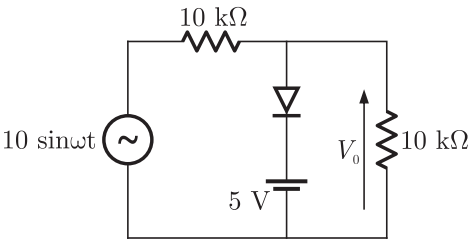


YEAR 2008 ONE MARK

MCQ 8.30 The equivalent circuits of a diode during forward biased and reverse biased conditions, are shown in the figure.

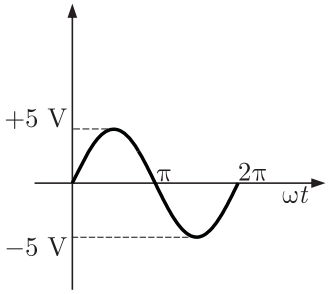
(I)

(II)

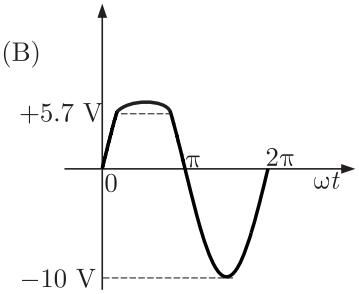


If such a diode is used in clipper circuit of figure given above, the output voltage V_0 of the circuit will be

(A)



(B)



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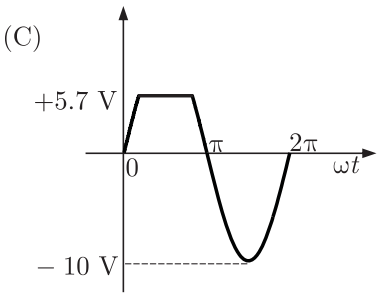
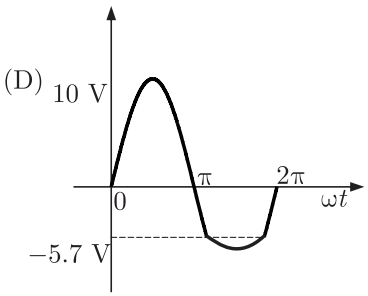
(C)

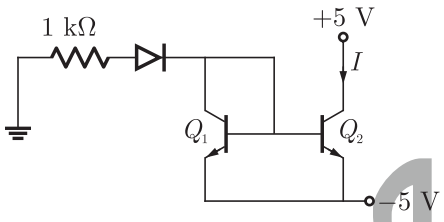


(D)



YEAR 2008 TWO MARKS

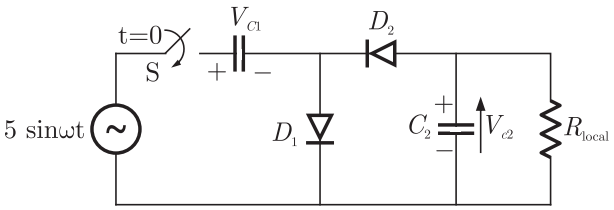
MCQ 8.31 Two perfectly matched silicon transistor are connected as shown in the figure assuming the β of the transistors to be very high and the forward voltage drop in diodes to be 0.7 V, the value of current I is



(A) 0 mA (B) 3.6 mA

(C) 4.3 mA (D) 5.7 mA

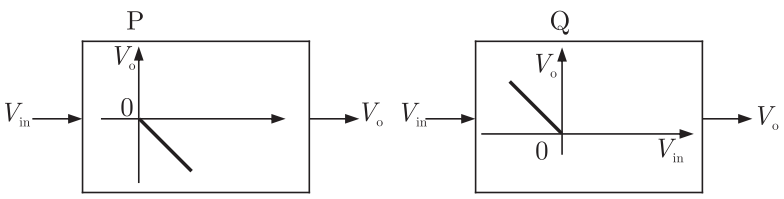
MCQ 8.32 In the voltage doubler circuit shown in the figure, the switch 'S' is closed at $t = 0$. Assuming diodes D_1 and D_2 to be ideal, load resistance to be infinite and initial capacitor voltages to be zero. The steady state voltage across capacitor C_1 and C_2 will be



(A) $V_{c1} = 10\text{ V}, V_{c2} = 5\text{ V}$ (B) $V_{c1} = 10\text{ V}, V_{c2} = -5\text{ V}$

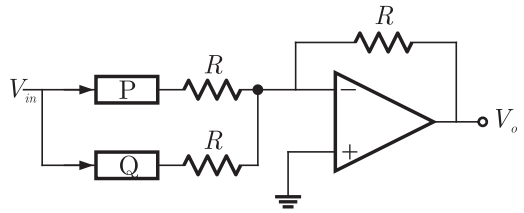
(C) $V_{c1} = 5\text{ V}, V_{c2} = 10\text{ V}$ (D) $V_{c1} = 5\text{ V}, V_{c2} = -10\text{ V}$

MCQ 8.33 The block diagrams of two of half wave rectifiers are shown in the figure. The transfer characteristics of the rectifiers are also shown within the block.

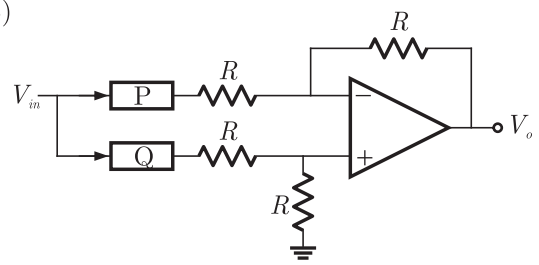


It is desired to make full wave rectifier using above two half-wave rectifiers. The resultants circuit will be

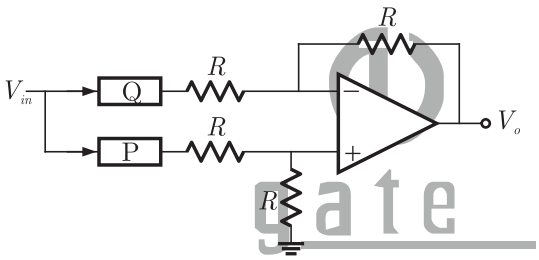
(A)



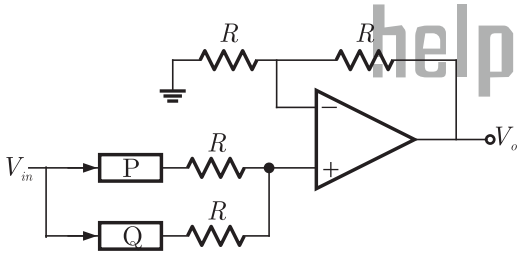
(B)



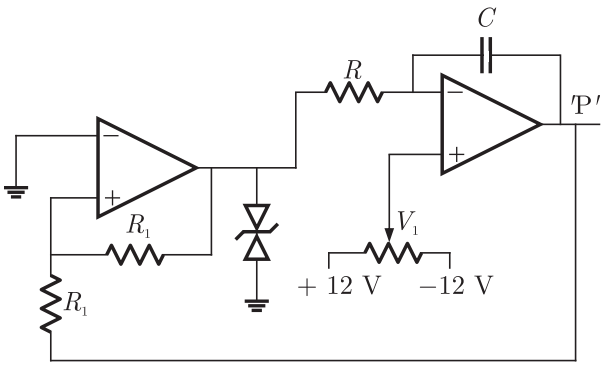
(C)



(D)



MCQ 8.34 A waveform generator circuit using OPAMPs is shown in the figure. It produces a triangular wave at point 'P' with a peak to peak voltage of 5 V for $V_i = 0$ V.



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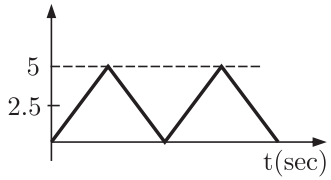
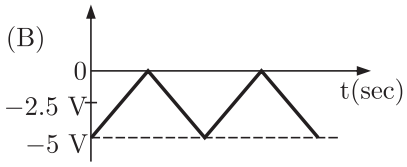
If the voltage V_i is made +2.5 V, the voltage waveform at point 'P' will become

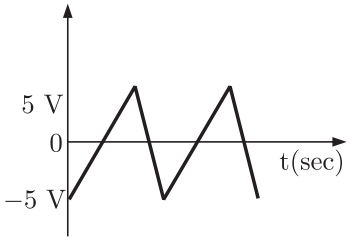
(A)



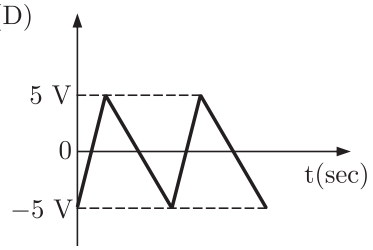
(B)



(C)

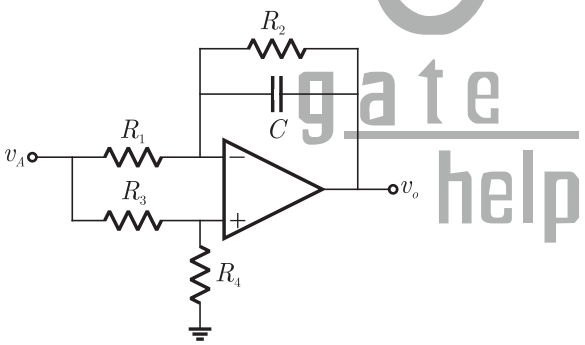


(D)



Statement for Linked Answer Questions 21 and 22.

A general filter circuit is shown in the figure :

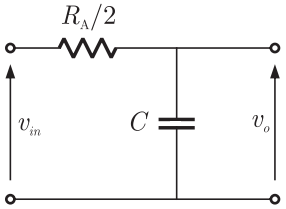


MCQ 8.35 If $R_1 = R_2 = R_A$ and $R_3 = R_4 = R_B$, the circuit acts as a

(A) all pass filter (B) band pass filter

(C) high pass filter (D) low pass filter

MCQ 8.36 The output of the filter in Q.21 is given to the circuit in figure : The gain v/s frequency characteristic of the output (v_o) will be



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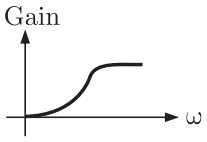
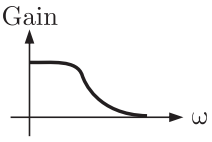
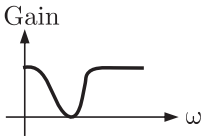
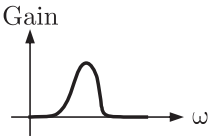
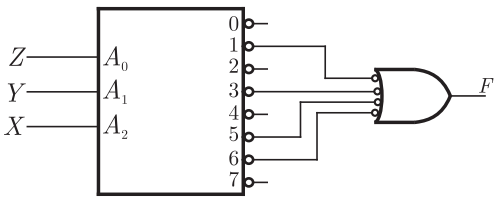
(A) 

(B) 

(C) 

(D) 

MCQ 8.37 A 3-line to 8-line decoder, with active low outputs, is used to implement a 3-variable Boolean function as shown in the figure



The simplified form of Boolean function $F(A, B, C)$ implemented in 'Product of Sum' form will be

(A) $(X+Z)(\overline{X}+\overline{Y}+\overline{Z})(Y+Z)$

(B) $(\overline{X}+\overline{Z})(X+Y+Z)(\overline{Y}+\overline{Z})$

(C) $(\overline{X}+\overline{Y}+Z)(\overline{X}+Y+Z)(X+\overline{Y}+Z)(X+Y+\overline{Z})$

(D) $(\overline{X}+\overline{Y}+Z)(\overline{X}+Y+\overline{Z})(X+\overline{Y}+Z)(X+\overline{Y}+\overline{Z})$

MCQ 8.38 The content of some of the memory location in an 8085 accumulator based system are given below

Address	Content
...	...
26FE	00
26FF	01
2700	02
2701	03
2702	04
...	...

The content of stack (SP), program counter (PC) and (H,L) are 2700 H, 2100 H and 0000 H respectively. When the following sequence of instruction are executed.

2100 H: DAD SP

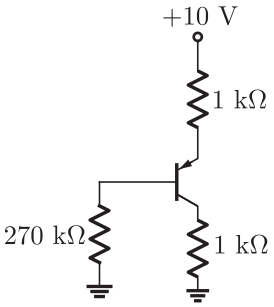
2101 H: PCHL

the content of (SP) and (PC) at the end of execution will be

(A) PC = 2102 H, SP = 2700 H
(B) PC = 2700 H, SP = 2700 H
(C) PC = 2800 H, SP = 26FE H
(D) PC = 2A02 H, SP = 2702 H

YEAR 2007 ONE MARK

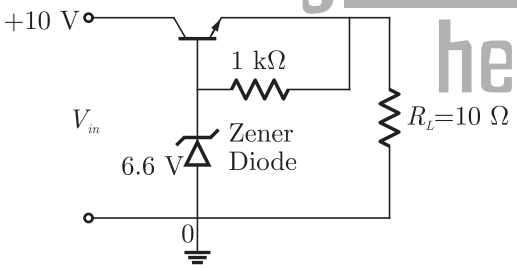
MCQ 8.39 The common emitter forward current gain of the transistor shown is $\beta_F = 100$



The transistor is operating in

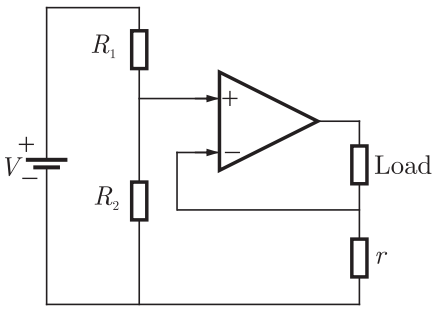
(A) Saturation region
(B) Cutoff region
(C) Reverse active region
(D) Forward active region

MCQ 8.40 The three-terminal linear voltage regulator is connected to a 10 Ω load resistor as shown in the figure. If V_{in} is 10 V, what is the power dissipated in the transistor ?



(A) 0.6 W
(B) 2.4 W
(C) 4.2 W
(D) 5.4 W

MCQ 8.41 The circuit shown in the figure is



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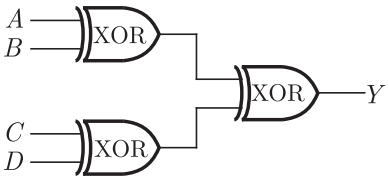
(A) a voltage source with voltage $\dfrac{rV}{R_1 \parallel R_2}$

(B) a voltage source with voltage $\dfrac{r \parallel R_2}{R_1} V$

(C) a current source with current $\left(\dfrac{r \parallel R_2}{R_1 + R_2}\right)\dfrac{V}{r}$

(D) a current source with current $\left(\dfrac{R_2}{R_1 + R_2}\right)\dfrac{V}{r}$

MCQ 8.42 A, B, C and D are input, and Y is the output bit in the XOR gate circuit of the figure below. Which of the following statements about the sum S of A, B, C, D and Y is correct ?



(A) S is always with zero or odd

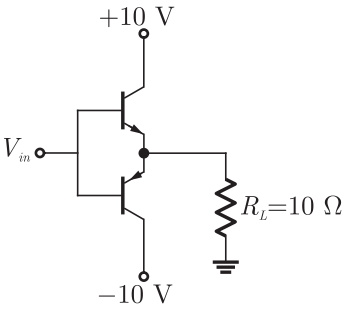
(B) S is always either zero or even

(C) $S = 1$ only if the sum of A, B, C and D is even

(D) $S = 1$ only if the sum of A, B, C and D is odd

YEAR 2007 **TWO MARKS**

MCQ 8.43 The input signal V_{in} shown in the figure is a 1 kHz square wave voltage that alternates between $+7$ V and -7 V with a 50% duty cycle. Both transistor have the same current gain which is large. The circuit delivers power to the load resistor R_L. What is the efficiency of this circuit for the given input ? choose the closest answer.



(A) 46%

(B) 55%

(C) 63%

(D) 92%

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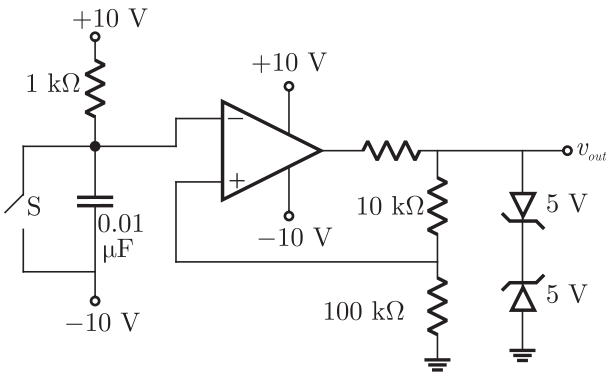
MCQ 8.44 The switch S in the circuit of the figure is initially closed, it is opened at time $t = 0$. You may neglect the zener diode forward voltage drops. What is the behavior of v_{out} for $t > 0$?



(A) It makes a transition from -5 V to $+5$ V at $t = 12.98\ \mu$s

(B) It makes a transition from -5 V to $+5$ V at $t = 2.57\ \mu$s

(C) It makes a transition from $+5$ V to -5 V at $t = 12.98\ \mu$s

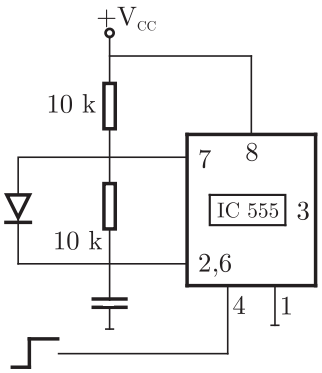
(D) It makes a transition from $+5$ V to -5 V at $t = 2.57\ \mu$s

MCQ 8.45 The Octal equivalent of HEX and number AB.CD is

(A) 253.314 (B) 253.632

(C) 526.314 (D) 526.632

MCQ 8.46 IC 555 in the adjacent figure is configured as an astable multi-vibrator. It is enabled to to oscillate at $t = 0$ by applying a high input to pin 4. The pin description is : 1 and 8-supply; 2-trigger; 4-reset; 6-threshold 7-discharge. The waveform appearing across the capacitor starting from $t = 0$, as observed on a storage CRO is



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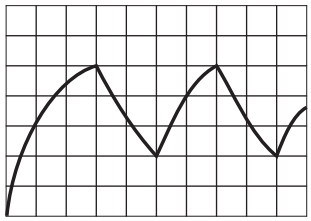
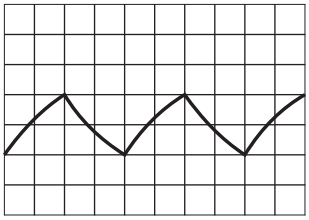
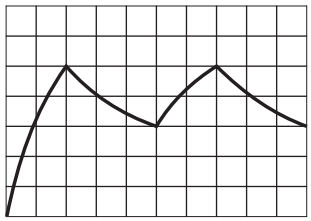
(A)



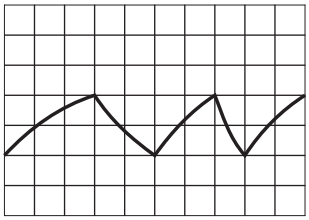
(B)



(C)

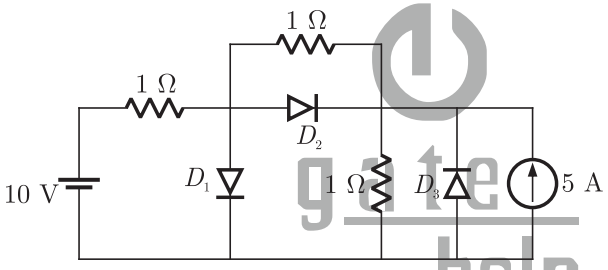


(D)



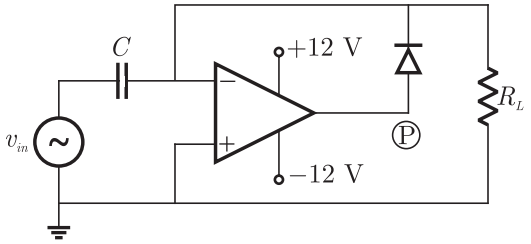
YEAR 2006 **ONE MARK**

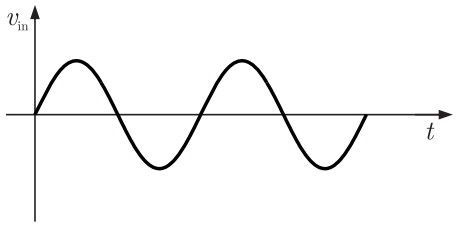
MCQ 8.47 What are the states of the three ideal diodes of the circuit shown in figure ?



(A) D_1 ON, D_2 OFF, D_3 OFF
(B) D_1 OFF, D_2 ON, D_3 OFF
(C) D_1 ON, D_2 OFF, D_3 ON
(D) D_1 OFF, D_2 ON, D_3 ON

MCQ 8.48 For a given sinusoidal input voltage, the voltage waveform at point P of the clamper circuit shown in figure will be





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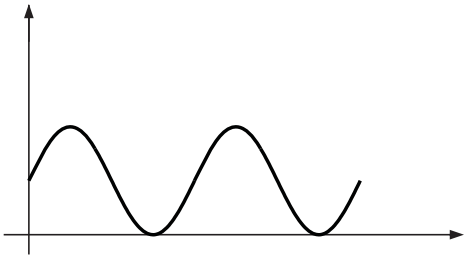
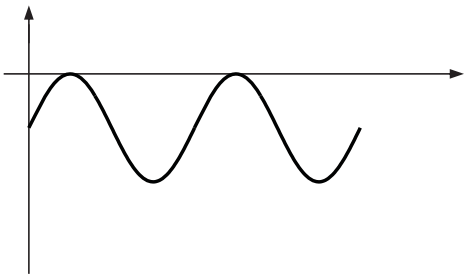
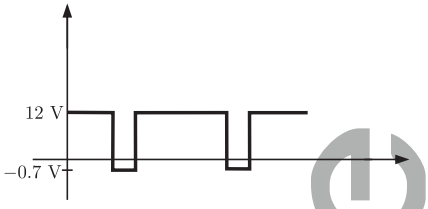
(A)



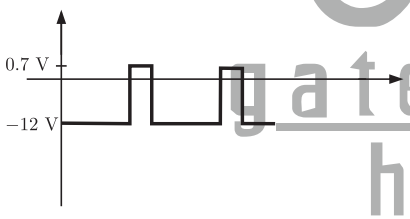
(B)



(C)



(D)



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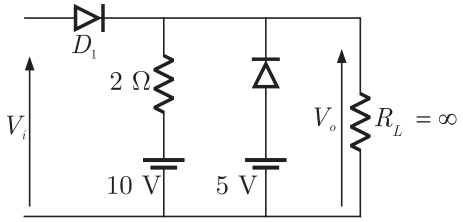
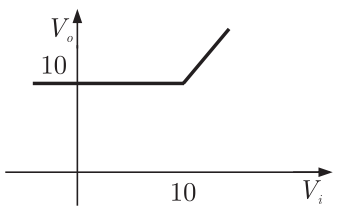
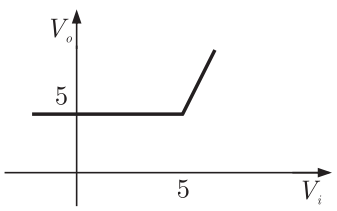
MCQ 8.49 Assuming the diodes D_1 and D_2 of the circuit shown in figure to be ideal ones, the transfer characteristics of the circuit will be



(A)



(B)



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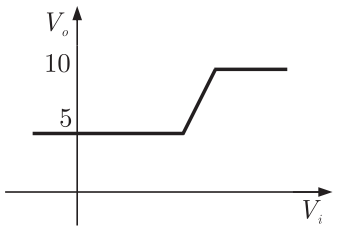
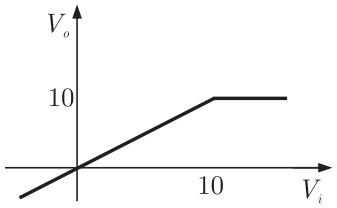
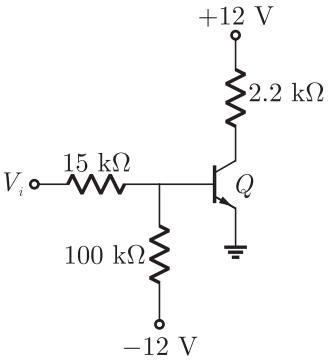
(C)



(D)

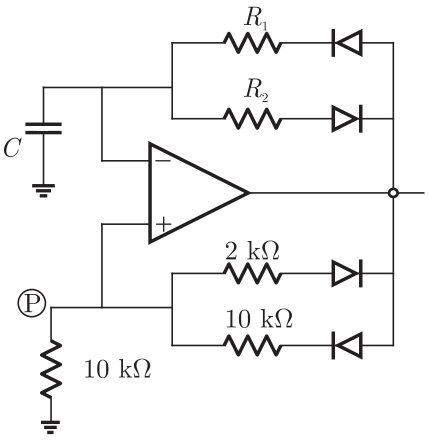


MCQ 8.50 Consider the circuit shown in figure. If the β of the transistor is 30 and I_{CBO} is 20 mA and the input voltage is $+5$ V, the transistor would be operating in

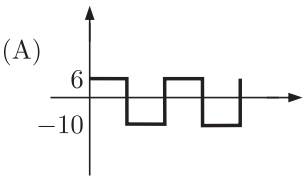


(A) saturation region
(B) active region
(C) breakdown region
(D) cut-off region

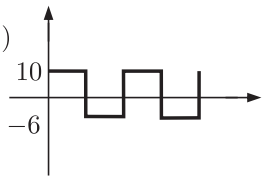
MCQ 8.51 A relaxation oscillator is made using OPAMP as shown in figure. The supply voltages of the OPAMP are ±12 V. The voltage waveform at point P will be



(A)



(B)



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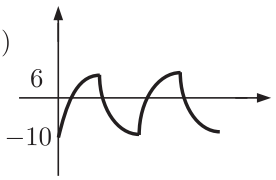
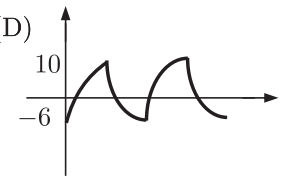
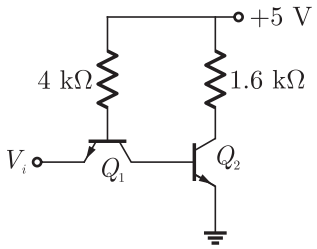
(C)



(D)



MCQ 8.52 A TTL NOT gate circuit is shown in figure. Assuming $V_{BE} = 0.7$ V of both the transistors, if $V_i = 3.0$ V, then the states of the two transistors will be



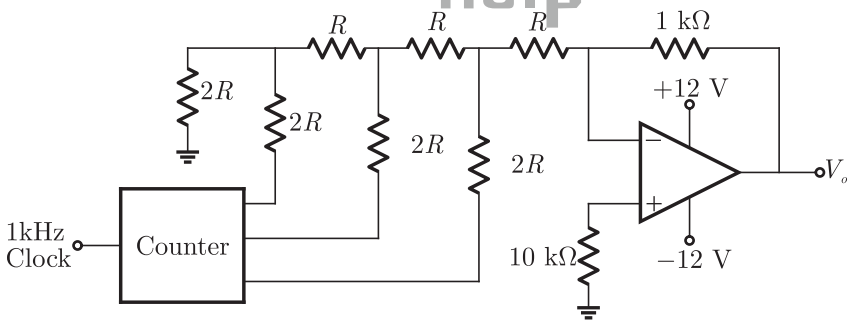
(A) Q_1 ON and Q_2 OFF

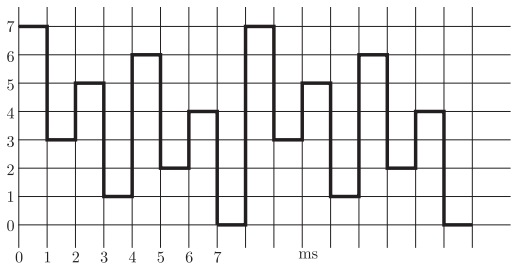
(B) Q_1 reverse ON and Q_2 OFF

(C) Q_1 reverse ON and Q_2 ON

(D) Q_1 OFF and Q_2 reverse ON

MCQ 8.53 A student has made a 3-bit binary down counter and connected to the R-$2R$ ladder type DAC, [Gain $= (-1\,\text{k}\Omega/2R)$] as shown in figure to generate a staircase waveform. The output achieved is different as shown in figure. What could be the possible cause of this error ?





(A) The resistance values are incorrect option.

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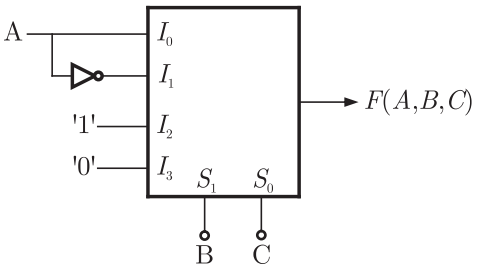
(B) The counter is not working properly

(C) The connection from the counter of DAC is not proper

(D) The R and 2R resistance are interchanged

MCQ 8.54 A 4×1 MUX is used to implement a 3-input Boolean function as shown in figure. The Boolean function $F(A,B,C)$ implemented is



(A) $F(A,B,C)=\Sigma(1,2,4,6)$ (B) $F(A,B,C)=\Sigma(1,2,6)$

(C) $F(A,B,C)=\Sigma(2,4,5,6)$ (D) $F(A,B,C)=\Sigma(1,5,6)$

MCQ 8.55 A software delay subroutine is written as given below :

```
DELAY :  MVI   H, 255D
         MVI   L, 255D
LOOP :   DCR   L
         JNZ   LOOP
         DCR   H
         JNZ   LOOP
```

How many times DCR L instruction will be executed ?

(A) 255 (B) 510

(C) 65025 (D) 65279

MCQ 8.56 In an 8085 A microprocessor based system, it is desired to increment the contents of memory location whose address is available in (D,E) register pair and store the result in same location. The sequence of instruction is

(A) XCHG
INR M

(B) XCHG
INX H

(C) INX D
XCHG

(D) INR M
XCHG

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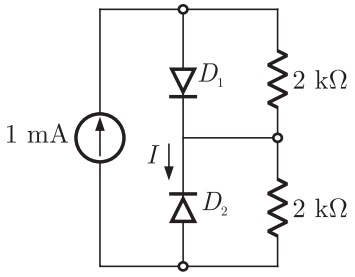
MCQ 8.57 Assume that D_1 and D_2 in figure are ideal diodes. The value of current is



(A) 0 mA (B) 0.5 mA

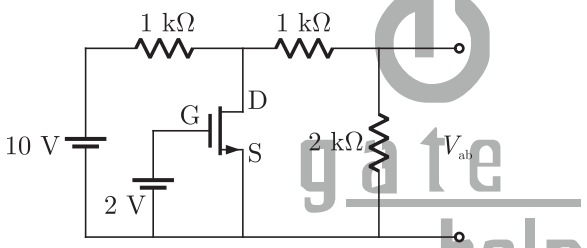
(C) 1 mA (D) 2 mA

MCQ 8.58 The 8085 assembly language instruction that stores the content of H and L register into the memory locations 2050_H and 2051_H, respectively is

(A) SPHL 2050_H (B) SPHL 2051_H

(C) SHLD 2050_H (D) STAX 2050_H

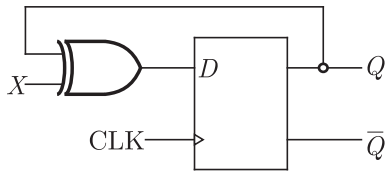
MCQ 8.59 Assume that the N-channel MOSFET shown in the figure is ideal, and that its threshold voltage is +1.0 V the voltage V_{ab} between nodes a and b is



(A) 5 V (B) 2 V

(C) 1 V (D) 0 V

MCQ 8.60 The digital circuit shown in the figure works as

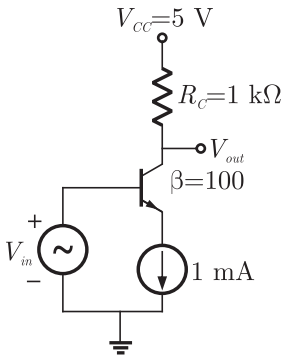


(A) JK flip-flop (B) Clocked RS flip-flop

(C) T flip-flop (D) Ring counter

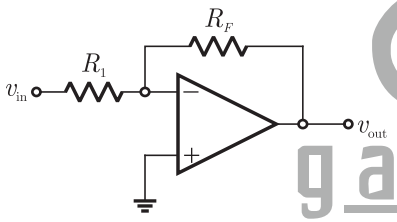
YEAR 2005 TWO MARKS

MCQ 8.61 The common emitter amplifier shown in the figure is biased using a 1 mA ideal current source. The approximate base current value is



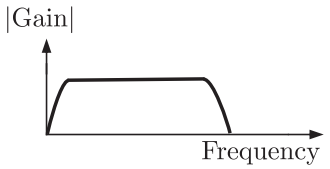
(A) 0 μA
(B) 10 μA
(C) 100 μA
(D) 1000 μA

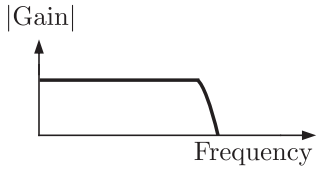
MCQ 8.62 Consider the inverting amplifier, using an ideal operational amplifier shown in the figure. The designer wishes to realize the input resistance seen by the small-signal source to be as large as possible, while keeping the voltage gain between -10 and -25. The upper limit on R_F is 1 MΩ. The value of R_1 should be

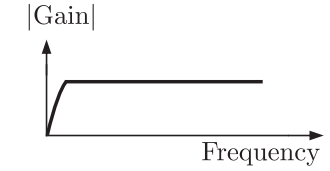


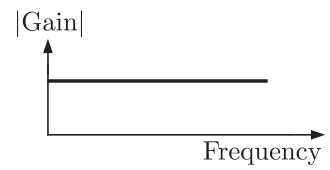
(A) Infinity
(B) 1 MΩ
(C) 100 kΩ
(D) 40 kΩ

MCQ 8.63 The typical frequency response of a two-stage direct coupled voltage amplifier is as shown in figure

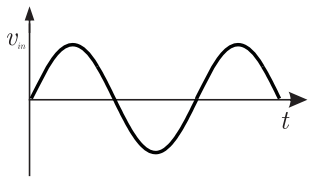
(A)


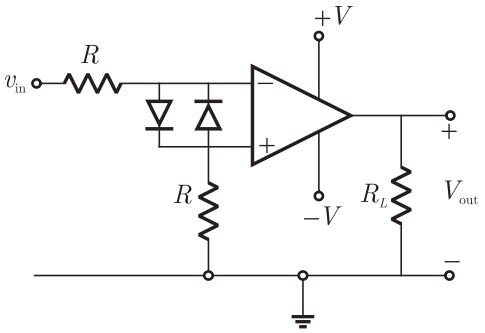
(B)


(C)


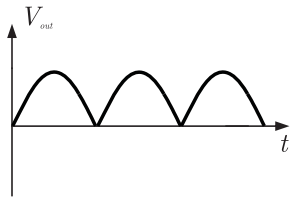
(D)


MCQ 8.64 In the given figure, if the input is a sinusoidal signal, the output will appear as shown

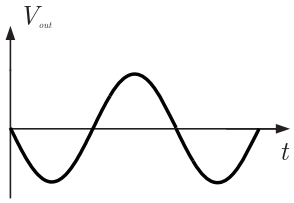




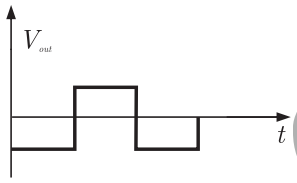
(A)



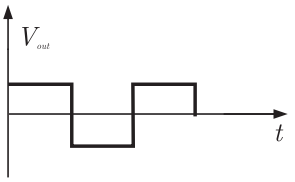
(B)



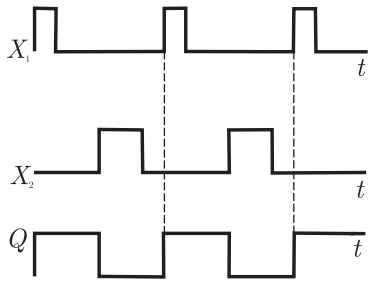
(C)



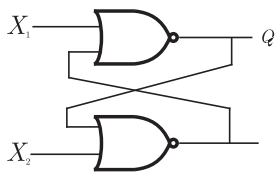
(D)



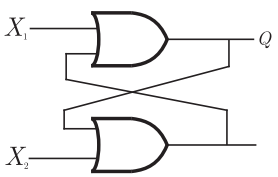
MCQ 8.65 Select the circuit which will produce the given output Q for the input signals X_1 and X_2 given in the figure



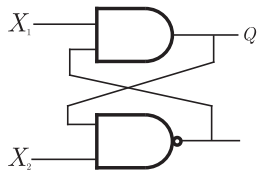
(A)



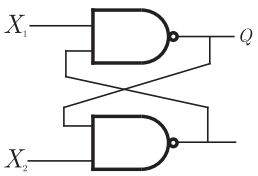
(B)



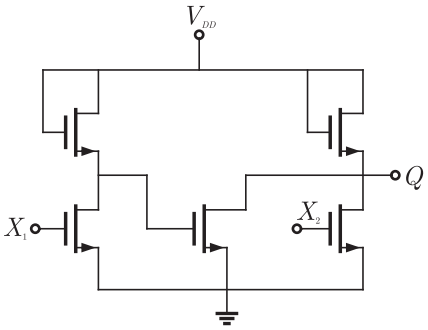
(C)



(D)



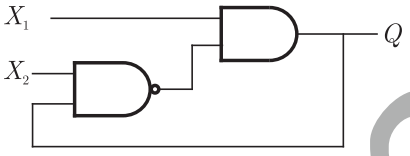
MCQ 8.66 If X_1 and X_2 are the inputs to the circuit shown in the figure, the output Q is



(A) $\overline{X_1 + X_2}$ (B) $\overline{X_1 \cdot X_2}$

(C) $\overline{X_1} \cdot X_2$ (D) $X_1 \cdot \overline{X_2}$

MCQ 8.67 In the figure, as long as $X_1 = 1$ and $X_2 = 1$, the output Q remains

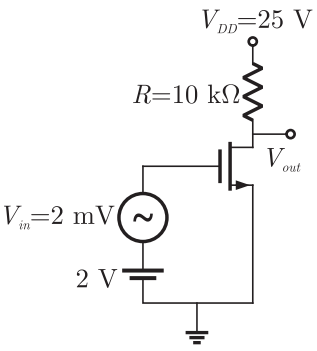


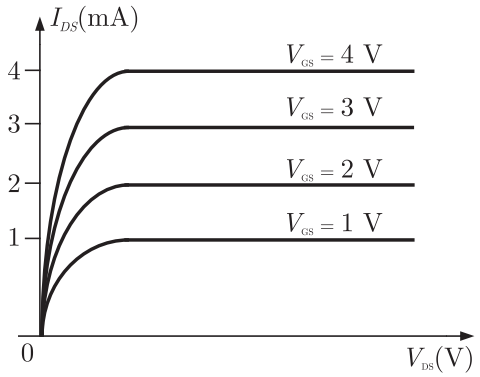
(A) at 1 (B) at 0

(C) at its initial value (D) unstable

Data for Q. 68 and Q. 69 are given below. Solve the problems and choose the correct option.

Assume that the threshold voltage of the N-channel MOSFET shown in figure is + 0.75 V. The output characteristics of the MOSFET are also shown





MCQ 8.68 The transconductance of the MOSFET is

(A) 0.75 ms (B) 1 ms

(C) 2 ms (D) 10 ms

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MCQ 8.69 The voltage gain of the amplifier is

(A) +5 (B) −7.5

(C) +10 (D) −10

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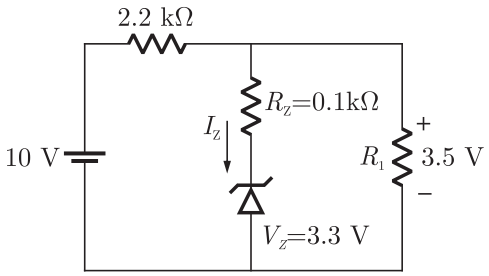
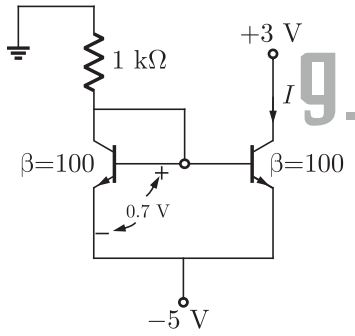
MCQ 8.70 The current through the Zener diode in figure is



(A) 33 mA (B) 3.3 mA

(C) 2 mA (D) 0 mA

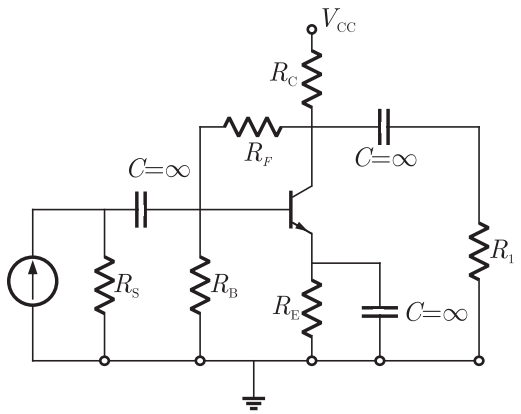
MCQ 8.71 Two perfectly matched silicon transistor are connected as shown in figure. The value of the current I is



(A) 0 mA (B) 2.3 mA

(C) 4.3 mA (D) 7.3 mA

MCQ 8.72 The feedback used in the circuit shown in figure can be classified as



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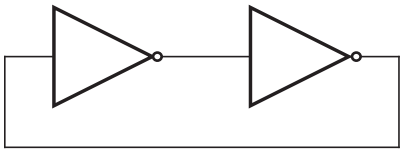
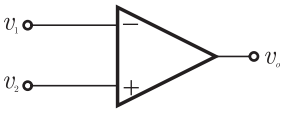
(A) shunt-series feedback
(B) shunt-shunt feedback
(C) series-shunt feedback
(D) series-series feedback

MCQ 8.73 The digital circuit using two inverters shown in figure will act as



(A) a bistable multi-vibrator
(B) an astable multi-vibrator
(C) a monostable multi-vibrator
(D) an oscillator

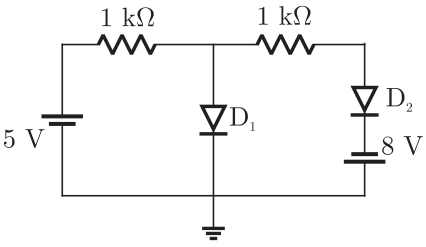
MCQ 8.74 The voltage comparator shown in figure can be used in the analog-to-digital conversion as



(A) a 1-bit quantizer
(B) a 2-bit quantizer
(C) a 4-bit quantizer
(D) a 8-bit quantizer

YEAR 2004 **TWO MARKS**

MCQ 8.75 Assuming that the diodes are ideal in figure, the current in diode D_1 is



(A) 9 mA
(B) 5 mA
(C) 0 mA
(D) −3 mA

MCQ 8.76 The trans-conductance g_m of the transistor shown in figure is 10 mS. The value of the input resistance R_{in} is

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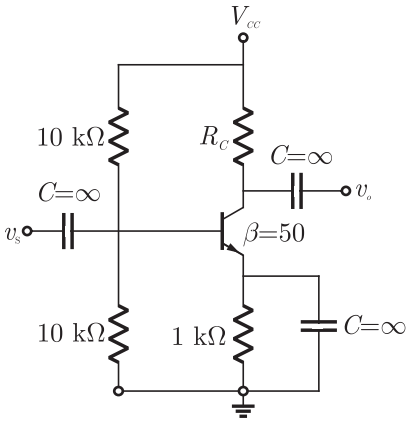
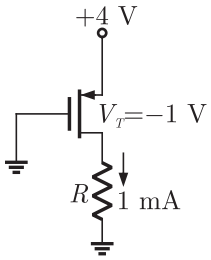


(A) 10.0 kΩ (B) 8.3 kΩ

(C) 5.0 kΩ (D) 2.5 kΩ

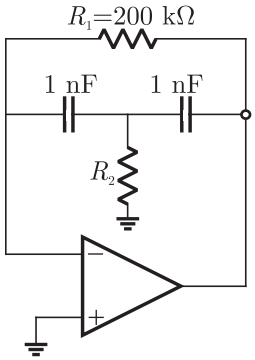
MCQ 8.77 The value of R for which the PMOS transistor in figure will be biased in linear region is



(A) 220 Ω (B) 470 Ω

(C) 680 Ω (D) 1200 Ω

MCQ 8.78 In the active filter circuit shown in figure, if Q = 1, a pair of poles will be realized with ω_0 equal to



(A) 1000 rad/s (B) 100 rad/s

(C) 10 rad/s (D) 1 rad/s

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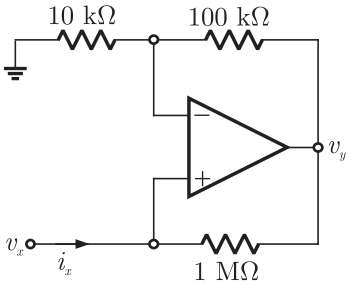
MCQ 8.79 The input resistance $R_{in} = v_x / i_x$ of the circuit in figure is

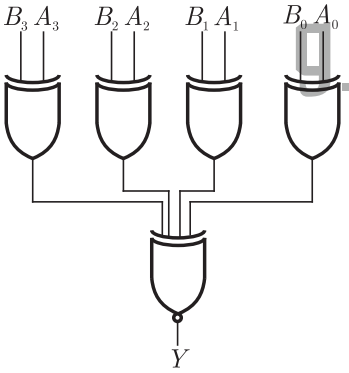


(A) $+100$ kΩ
(B) -100 kΩ
(C) $+1$ MΩ
(D) -1 MΩ

MCQ 8.80 The simplified form of the Boolean expression $Y = (\overline{A} \cdot BC + D)(\overline{A} \cdot D + \overline{B} \cdot \overline{C})$ can be written as

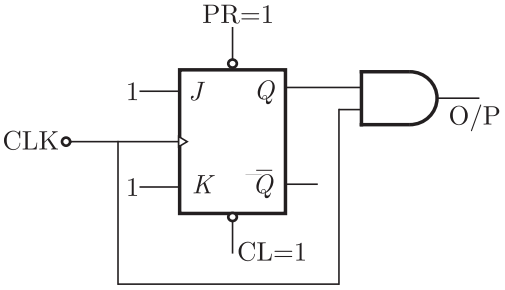
(A) $\overline{A} \cdot D + \overline{B} \cdot \overline{C} \cdot D$
(B) $AD + B \cdot \overline{C} \cdot D$
(C) $(\overline{A} + D)(\overline{B} \cdot C + \overline{D})$
(D) $A \cdot \overline{D} + BC \cdot \overline{D}$

MCQ 8.81 A digit circuit which compares two numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$ is shown in figure. To get output $Y = 0$, choose one pair of correct input numbers.



(A) 1010, 1010
(B) 0101, 0101
(C) 0010, 0010
(D) 1010, 1011

MCQ 8.82 The digital circuit shown in figure generates a modified clock pulse at the output. Choose the correct output waveform from the options given below.



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CLK 

(A) 

(B) 

(C) 

(D) 

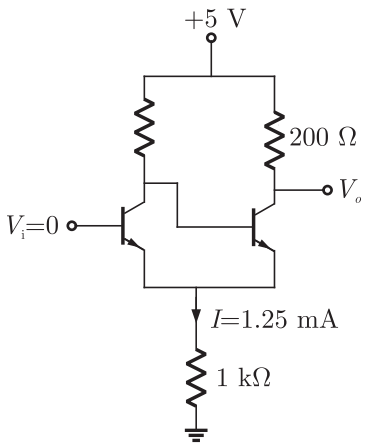
MCQ 8.83 If the following program is executed in a microprocessor, the number of instruction cycle it will take from START to HALT is

```
START   MVI A, 14H  ;  Move 14 H to register A
SHIFT   RLC         ;  Rotate left without carry
        JNZ SHIFT   ;  Jump on non-zero to SHIFT
        HALT
```

(A) 4 (B) 8

(C) 13 (D) 16

MCQ 8.84 In the Schmitt trigger circuit shown in figure, if $V_{CE(\text{sat})} = 0.1\,\text{V}$, the output logic low level (V_{OL}) is



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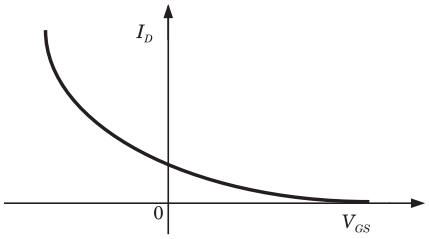
(A) 1.25 V (B) 1.35 V
(C) 2.50 V (D) 5.00 V

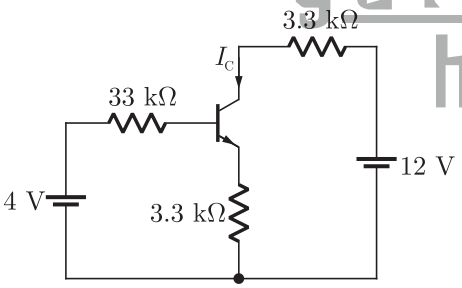
YEAR 2003 ONE MARK

MCQ 8.85 The variation of drain current with gate-to-source voltage ($I_D - V_{GS}$ characteristic) of a MOSFET is shown in figure. The MOSFET is



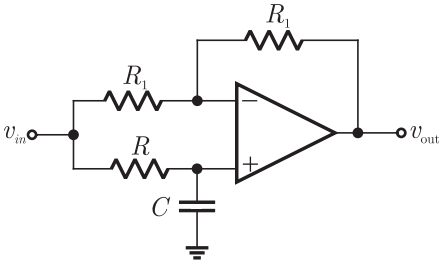
(A) an n-channel depletion mode device
(B) an n-channel enhancement mode device
(C) an p-channel depletion mode device
(D) an p-channel enhancement mode device

MCQ 8.86 In the circuit of figure, assume that the transistor has $h_{fe} = 99$ and $V_{BE} = 0.7$ V. The value of collector current I_C of the transistor is approximately



(A) [3.3/3.3] mA (B) [3.3/(3.3+3.3)] mA
(C) [3.3/.33] mA (D) [3.3(33+3.3)] mA

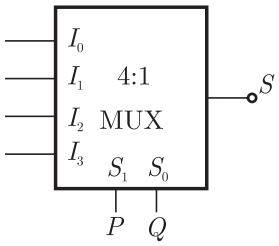
MCQ 8.87 For the circuit of figure with an ideal operational amplifier, the maximum phase shift of the output v_{out} with reference to the input v_{in} is



(A) 0° (B) -90°

(C) $+90^\circ$ (D) $\pm 180^\circ$

MCQ 8.88 Figure shows a 4 to 1 MUX to be used to implement the sum S of a 1-bit full adder with input bits P and Q and the carry input C_{in}. Which of the following combinations of inputs to I_0, I_1, I_2 and I_3 of the MUX will realize the sum S ?



(A) $I_0 = I_1 = C_{in}; I_2 = I_3 = \overline{C}_{in}$ (B) $I_0 = I_1 = \overline{C}_{in}; I_2 = I_3 = C_{in}$

(C) $I_0 = I_3 = C_{in}; I_1 = I_2 = \overline{C}_{in}$ (D) $I_0 = I_3 = \overline{C}_{in}; I_1 = I_2 = C_{in}$

MCQ 8.89 When a program is being executed in an 8085 microprocessor, its Program Counter contains

(A) the number of instructions in the current program that have already been executed

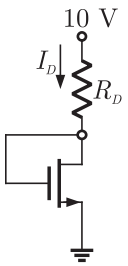
(B) the total number of instructions in the program being executed.

(C) the memory address of the instruction that is being currently executed

(D) the memory address of the instruction that is to be executed next

YEAR 2003 **TWO MARKS**

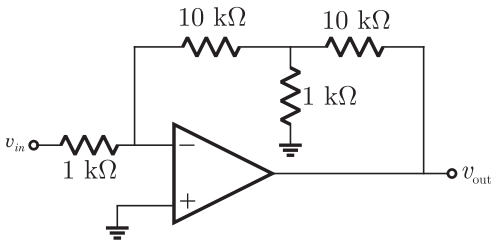
MCQ 8.90 For the n-channel enhancement MOSFET shown in figure, the threshold voltage $V_{th} = 2$ V. The drain current I_D of the MOSFET is 4 mA when the drain resistance R_D is 1 kΩ.If the value of R_D is increased to 4 kΩ, drain current I_D will become



(A) 2.8 mA (B) 2.0 mA

(C) 1.4 mA (D) 1.0 mA

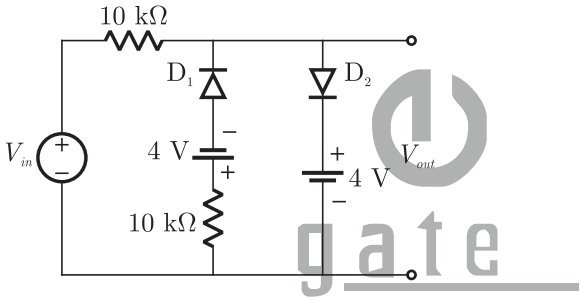
MCQ 8.91 Assuming the operational amplifier to be ideal, the gain v_{out}/v_{in} for the circuit shown in figure is



(A) -1 (B) -20

(C) -100 (D) -120

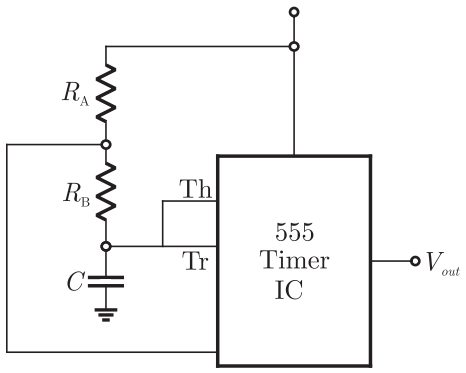
MCQ 8.92 A voltage signal $10\sin\omega t$ is applied to the circuit with ideal diodes, as shown in figure, The maximum, and minimum values of the output waveform V_{out} of the circuit are respectively



(A) $+10$ V and -10 V (B) $+4$ V and -4 V

(C) $+7$ V and -4 V (D) $+4$ V and -7 V

MCQ 8.93 The circuit of figure shows a 555 Timer IC connected as an astable multivibrator. The value of the capacitor C is 10 nF. The values of the resistors R_A and R_B for a frequency of 10 kHz and a duty cycle of 0.75 for the output voltage waveform are



(A) $R_A = 3.62\,\text{k}\Omega, R_B = 3.62\,\text{k}\Omega$

(B) $R_A = 3.62\,\text{k}\Omega, R_B = 7.25\,\text{k}\Omega$

(C) $R_A = 7.25\,\text{k}\Omega, R_B = 3.62\,\text{k}\Omega$

(D) $R_A = 7.25\,\text{k}\Omega, R_B = 7.25\,\text{k}\Omega$

MCQ 8.94 The boolean expression $\overline{X}\,Y\,\overline{Z} + \overline{XYZ} + XY\overline{Z} + X\overline{Y}Z + XYZ$ can be simplified to

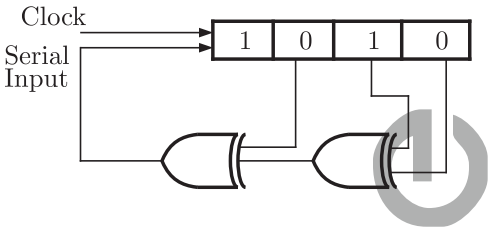
(A) $X\overline{Z} + \overline{X}Z + YZ$

(B) $XY + \overline{Y}Z + Y\overline{Z}$

(C) $\overline{X}Y + YZ + XZ$

(D) $\overline{XY} + Y\overline{Z} + \overline{X}Z$

MCQ 8.95 The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (msb). After how many clock pulses will the content of the shift register become 1010 again ?



(A) 3

(B) 7

(C) 11

(D) 15

MCQ 8.96 An X-Y flip-flop, whose Characteristic Table is given below is to be implemented using a J-K flip flop

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	$\overline{Q}_n$
1	1	0

(A) $J = X, K = \overline{Y}$

(B) $J = \overline{X}, K = Y$

(C) $J = Y, K = \overline{X}$

(D) $J = \overline{Y}, K = X$

MCQ 8.97 A memory system has a total of 8 memory chips each with 12 address lines and 4 data lines, The total size of the memory system is

(A) 16 kbytes

(B) 32 kbytes

(C) 48 kbytes

(D) 64 kbytes

MCQ 8.98 The following program is written for an 8085 microprocessor to add two bytes located at memory addresses 1FFE and 1FFF

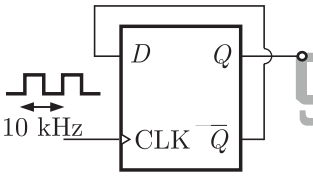
```
LXI   H, 1FFE
MOV   B, M
INR   L
MOV   A, M
ADD   B
INR   L
MOV   M, A
XOR   A
```

On completion of the execution of the program, the result of addition is found

(A) in the register A
(B) at the memory address 1000
(C) at the memory address 1F00
(D) at the memory address 2000

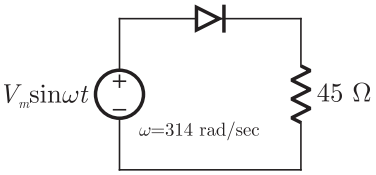
YEAR 2002 **ONE MARK**

MCQ 8.99 The frequency of the clock signal applied to the rising edge triggered D-flip-flop shown in Figure is 10 kHz. The frequency of the signal available at Q is.



(A) 10 kHz
(B) 2.5 kHz
(C) 20 kHz
(D) 5 kHz

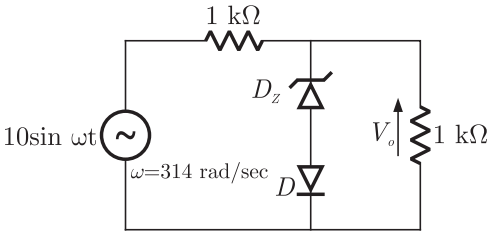
MCQ 8.100 The forward resistance of the diode shown in Figure is 5 Ω and the remaining parameters are same at those of an ideal diode. The dc component of the source current is



(A) $\frac{V_m}{50\pi}$
(B) $\frac{V_m}{50\pi\sqrt{2}}$
(C) $\frac{V_m}{100\pi\sqrt{2}}$
(D) $\frac{2V_m}{50\pi}$

MCQ 8.101 The cut-in voltage of both zener diode D_Z and diode D shown in Figure is 0.7 V, while break-down voltage of D_Z is 3.3 V and reverse break-down voltage of D is 50 V. The other parameters can be assumed to be the same

as those of an ideal diode. The values of the peak output voltage (V_o) are



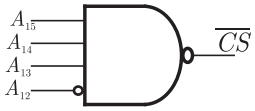
(A) 3.3 V in the positive half cycle and 1.4 V in the negative half cycle.

(B) 4 V in the positive half cycle and 5 V in the negative half cycle.

(C) 3.3 V in both positive and negative half cycles.

(D) 4 V in both positive and negative half cycle

MCQ 8.102 The logic circuit used to generate the active low chip select ($\overline{CS}$) by an 8085 microprocessor to address a peripheral is shown in Figure. The peripheral will respond to addresses in the range.



(A) E000-EFFF

(B) 000E-FFFE

(C) 1000-FFFF

(D) 0001-FFF1

YEAR 2002 **TWO MARKS**

MCQ 8.103 A first order, low pass filter is given with $R = 50\,\Omega$ and $C = 5\,\mu$F. What is the frequency at which the gain of the voltage transfer function of the filter is 0.25 ?

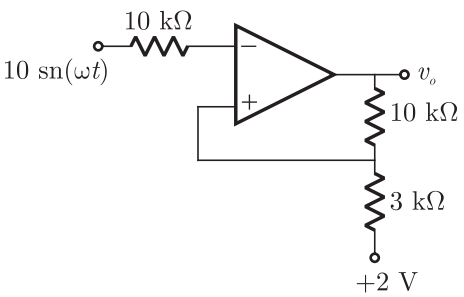
(A) 4.92 kHz

(B) 0.49 kHz

(C) 2.46 kHz

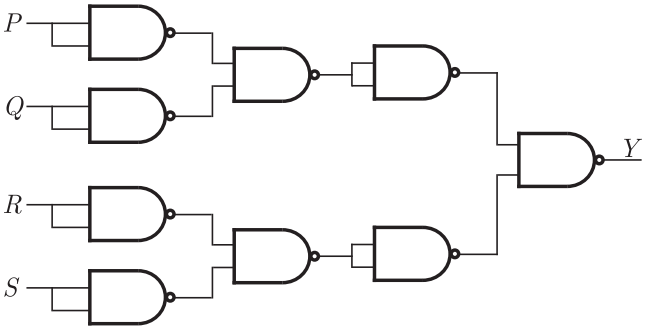
(D) 24.6 kHz

MCQ 8.104 The output voltage (v_o) of the Schmitt trigger shown in Figure swings between $+15$ V and -15 V. Assume that the operational amplifier is ideal. The output will change from $+15$ V to -15 V when the instantaneous value of the input sine wave is



(A) 5 V in the positive slope only
(B) 5 V in the negative slope only
(C) 5 V in the positive and negative slopes
(D) 3 V in the positive and negative slopes.

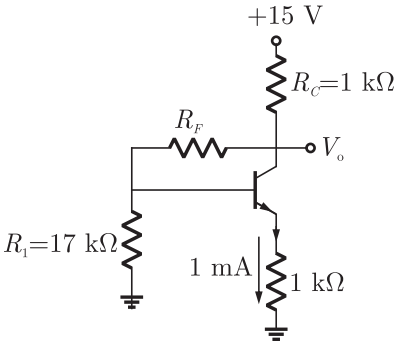
MCQ 8.105 For the circuit shown in Figure, the boolean expression for the output Y in terms of inputs P, Q, R and S is



(A) $\overline{P}+\overline{Q}+\overline{R}+\overline{S}$
(B) $P+Q+R+S$
(C) $(\overline{P}+\overline{Q})(\overline{R}+\overline{S})$
(D) $(P+Q)(R+S)$

Common Data Questions Q.106-108*

For the circuit shown in Figure, $I_E = 1$ mA, $\beta = 99$ and $V_{BE} = 0.7$ V



MCQ 8.106 The current through R_C is
(A) 0.99 mA
(B) 1.1 mA
(C) 1.20 mA
(D) 1 mA

MCQ 8.107 Output voltage V_0 will be
(A) 16.1 Volt
(B) 14 Volt
(C) 13.9 Volt
(D) None of these

MCQ 8.108 Value of resistance R_F is

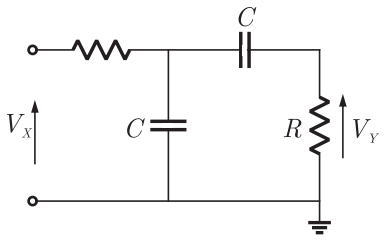
(A) 110.9 kΩ (B) 124.5 kΩ

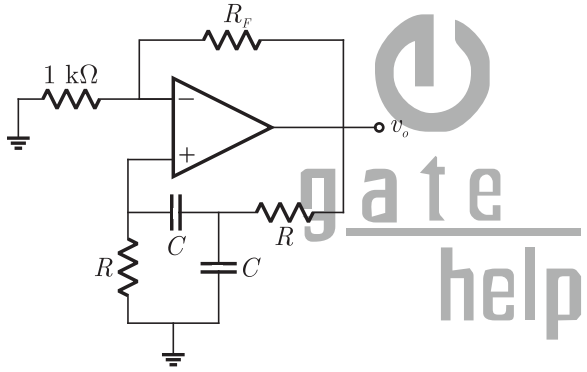
(C) 130.90 kΩ (D) None of these

Common data question Q.95-97*.

The following network is used as a feedback circuit in an oscillator shown in figure to generate sinusoidal oscillations. Assuming that the operation amplifier is ideal.

given that $R = 10\,\text{k}\Omega$ and $C = 100\,\text{pF}$





MCQ 8.109 The transfer function $\frac{V_y}{V_x}$ of the first network is

(A) $\frac{j\omega CR}{(1-\omega^2 R^2 C^2)+j3\omega CR}$ (B) $\frac{j\omega CR}{(1-\omega^2 R^2 C^2)+j2\omega CR}$

(C) $\frac{j\omega CR}{1+j3\omega CR}$ (D) $\frac{j\omega CR}{1+j2\omega CR}$

MCQ 8.110 The frequency of oscillation will be

(A) $\frac{1}{RC}$ (B) $\frac{1}{2RC}$

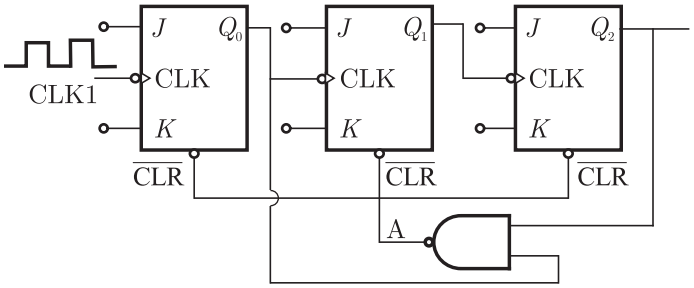
(C) $\frac{1}{4RC}$ (D) None of these

MCQ 8.111 Value of R_F is

(A) 1 kΩ (B) 4 kΩ

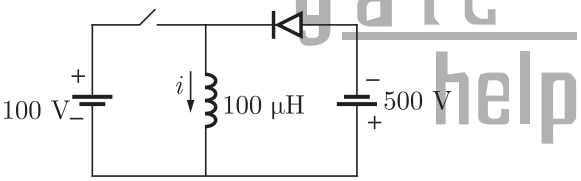
(C) 2 kΩ (D) 8 kΩ

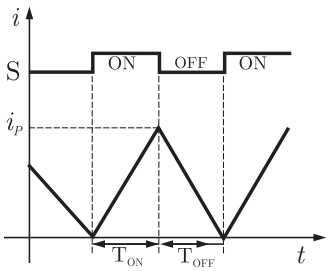
MCQ 8.112 *The ripple counter shown in figure is made up of negative edge triggered J-K flip-flops. The signal levels at J and K inputs of all the flip flops are maintained at logic 1. Assume all the outputs are cleared just prior to applying the clock signal.
module no. of the counter is:



(A) 7 (B) 5
(C) 4 (D) 8

MCQ 8.113 *In Figure , the ideal switch S is switched on and off with a switching frequency $f = 10$ kHz. The switching time period is $T = t_{ON} + t_{OFF}$ μs. The circuit is operated in steady state at the boundary of continuous and discontinuous conduction, so that the inductor current i is as shown in Figure. Values of the on-time t_{ON} of the switch and peak current i_p. are



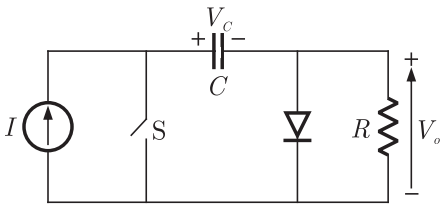


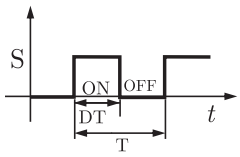
(A) 63.33 μsec, 63.33 A (B) 63.33 μsec, 63.33 μA
(C) 66.66 μsec, 66.66 mA (D) none of these

Common Data Questions Q.114-115*

In the circuit shown in Figure, the source I is a dc current source.The switch S is operated with a time period T and a duty ratio D. You may assume

that the capacitance C has a finite value which is large enough so that the voltage. V_C has negligible ripple, calculate the following under steady state conditions, in terms of D, I and R





MCQ 8.114 The voltage V_c, with the polarity shown in Figure,

(A) $\frac{I}{C}$ (B) $\frac{I}{C}(1-DT)$

(C) $\frac{I}{C}(1-D)\,T$ (D) $-\frac{I}{C}\,T$

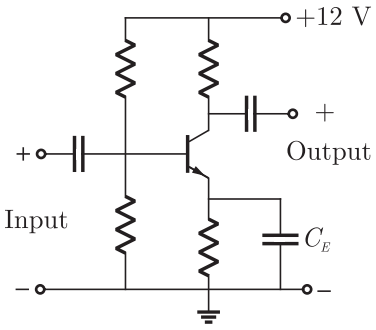
MCQ 8.115 The average output voltage V_0, with the polarity shown in figure

(A) $-\frac{I}{C}\,T$ (B) $-\frac{I}{2C}D^2\,T$

(C) $\frac{I}{2C}(1-DT)$ (D) $\frac{I}{2C}(1-D)\,T$

YEAR 2001 ONE MARK

MCQ 8.116 In the single-stage transistor amplifier circuit shown in Figure, the capacitor C_E is removed. Then, the ac small-signal mid-band voltage gain of the amplifier



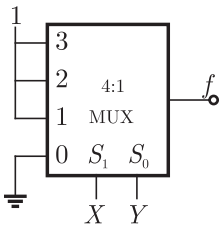
(A) increase (B) decreases

(C) is unaffected (D) drops to zero

MCQ 8.117 Among the following four, the slowest ADC (analog-to-digital converter) is
(A) parallel-comparator (i.e. flash) type
(B) successive approximation type
(C) integrating type
(D) counting type

MCQ 8.118 The output of a logic gate is "1" when all its inputs are at logic "0". The gate is either
(A) a NAND or an EX-OR gate
(B) a NOR or an EX-OR gate
(C) an AND or an EX-NOR gate
(D) a NOR or an EX-NOR gate

MCQ 8.119 The output f of the 4-to-1 MUX shown in Figure is

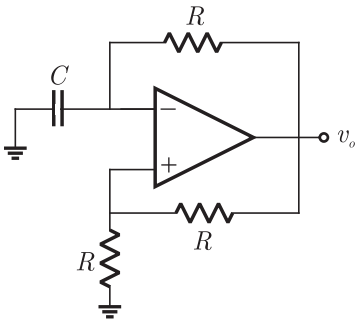


(A) $\overline{xy}+x$ (B) $x+y$
(C) $\overline{x}+\overline{y}$ (D) $xy+\overline{x}$

MCQ 8.120 An op-amp has an open-loop gain of 10^5 and an open-loop upper cut-off frequency of 10 Hz. If this op-amp is connected as an amplifier with a closed-loop gain of 100, then the new upper cut-off frequency is
(A) 10 Hz (B) 100 Hz
(C) 10 kHz (D) 100 kHz

YEAR 2001 TWO MARKS

MCQ 8.121 For the oscillator circuit shown in Figure, the expression for the time period of oscillation can be given by (where $\tau = RC$)



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(A) $\tau \ln 3$ (B) $2\tau \ln 3$

(C) $\tau \ln 2$ (D) $2\tau \ln 2$

MCQ 8.122 An Intel 8085 processor is executing the program given below.

```
        MVI A, 10 H
        MVI B, 10 H
BACK:   NOP
        ADD B
        RLC
        INC BACK
        HLT
```

The number of times that the operation NOP will be executed is equal to

(A) 1 (B) 2

(C) 3 (D) 4

MCQ 8.123 A sample-and-hold (S/H) circuit, having a holding capacitor of 0.1 nF, is used at the input of an ADC (analog-to-digital converter). The conversion time of the ADC is 1 μsec, and during this time, the capacitor should not loose more than 0.5% of the charge put across it during the sampling time. The maximum value of the input signal to the S/H circuit is 5 V. The leakage current of the S/H circuit should be less than

(A) 2.5 mA (B) 0.25 mA

(C) 25.0 μA (D) 2.5 μA

MCQ 8.124 An op-amp, having a slew rate of 62.8 V/μsec, is connected in a voltage follower configuration. If the maximum amplitude of the input sinusoidal is 10 V, then the minimum frequency at which the slew rate limited distortion would set in at the output is

(A) 1.0 MHz (B) 6.28 MHz

(C) 10.0 MHz (D) 62.8 MHz

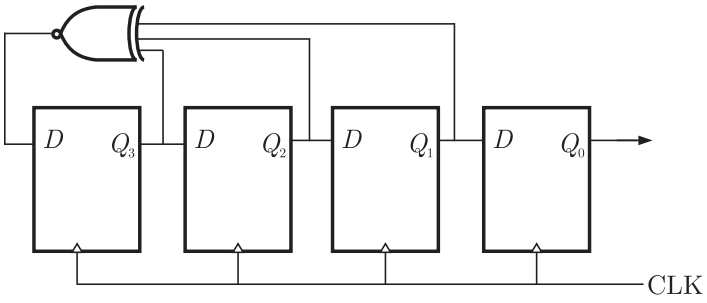
MCQ 8.125 An n-channel JFET, having a pinch off voltage (V_p) of -5 V, shows a transconductance (g_m) of 1 mA/V when the applied gate -to-source voltage (V_{GS}) is -3 V. Its maximum transconductance (in mA/V) is

(A) 1.5 (B) 2.0

(C) 2.5 (D) 3.0

MCQ 8.126 *The circuit shown in the figure is a MOD-N ring counter. Value of N is

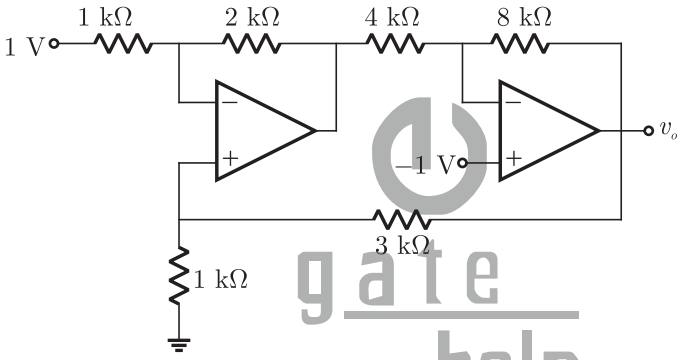
(assume initial state of the counter is 1110 i.e. $Q_3\,Q_2\,Q_1\,Q_0 = 1110$).



(A) 4 (B) 15

(C) 7 (D) 6

MCQ 8.127 *For the op-amp circuit shown in Figure, determine the output voltage v_o. Assume that the op-amps are ideal.

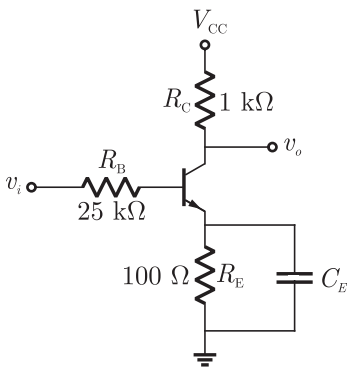


(A) $-\frac{8}{7}$ V (B) $-\frac{20}{7}$ V

(C) -10 V (D) None of these

Common Data Questions Q.128-129*.

The transistor in the amplifier circuit shown in Figure is biased at $I_C = 1\,\text{mA}$ Use $V_T = kT/q = 26\,\text{mV}, \beta_0 = 200, r_b = 0$, and $r_0 \to \infty$



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MCQ 8.128 Small-signal mid-band voltage gain v_o/v_i is

(A) -8 (B) 38.46

(C) -6.62 (D) -1

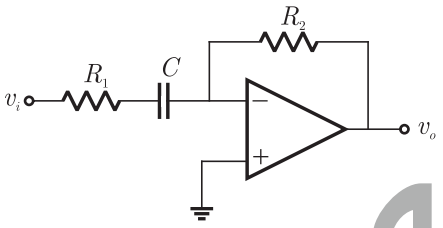
MCQ 8.129 What is the required value of C_E for the circuit to have a lower cut-off frequency of 10 Hz

(A) 0.15 mF (B) 1.59 mF

(C) 5 μF (D) 10 μF

Common Data Questions Q.130-131*

For the circuit shown in figure



MCQ 8.130 The circuit shown is a

(A) Low pass filter (B) Band pass filter

(C) Band Reject filter (D) High pass filter

MCQ 8.131 If the above filter has a 3 dB frequency of 1 kHz, a high frequency input resistance of 100 kΩ and a high frequency gain of magnitude 10. Then values of R_1, R_2 and C respectively are :-

(A) 100 kΩ, 1000 kΩ, 15.9 nF

(B) 10 kΩ, 100 kΩ, 0.11 μF

(C) 100 kΩ, 1000 kΩ, 15.9 nF

(D) none of these

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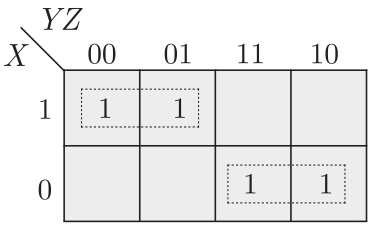
SOLUTION

SOL 8.1 Option (A) is correct.

Prime implicants are the terms that we get by solving K-map



$$F = \underbrace{X\overline{Y} + \overline{X}Y}_{\text{prime implicants}}$$

SOL 8.2 Option (D) is correct.

Let $v > 0.7$ V and diode is forward biased. Applying Kirchoff's voltage law

$$10 - i \times 1\text{k} - v = 0$$

$$10 - \left[\frac{v - 0.7}{500}\right](1000) - v = 0$$

$$10 - (v - 0.7) \times 2 - v = 0$$

$$v = \frac{11.4}{3} = 3.8\text{ V} > 0.7 \qquad \text{(Assumption is true)}$$

So, $$i = \frac{v - 0.7}{500} = \frac{3.8 - 0.7}{500} = 6.2\text{ mA}$$

SOL 8.3 Option (B) is correct.

$Y = 1$, when $A > B$

$$A = a_1 a_0,\ B = b_1 b_0$$

a_1	a_0	b_1	b_0	Y
0	1	0	0	1
1	0	0	0	1
1	0	0	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1

Total combination = 6

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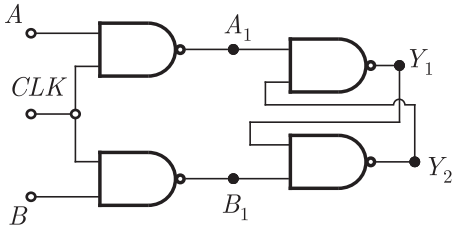
SOL 8.4 Option (A) is correct.

The given circuit is



Condition for the race-around

It occurs when the output of the circuit (Y_1, Y_2) oscillates between '0' and '1' checking it from the options.

1. Option (A): When $CLK = 0$

Output of the NAND gate will be $A_1 = B_1 = \overline{0} = 1$. Due to these input to the next NAND gate, $Y_2 = \overline{Y_1 \cdot 1} = \overline{Y_1}$ and $Y_1 = \overline{Y_2 \cdot 1} = \overline{Y_2}$.

If $Y_1 = 0$, $Y_2 = \overline{Y_1} = 1$ and it will remain the same and doesn't oscillate.

If $Y_2 = 0$, $Y_1 = \overline{Y_2} = 1$ and it will also remain the same for the clock period. So, it won't oscillate for $CLK = 0$.

So, here race around doesn't occur for the condition $CLK = 0$.

2. Option (C): When $CLK = 1$, $A = B = 1$

$A_1 = B_1 = 0$ and so $Y_1 = Y_2 = 1$

And it will remain same for the clock period. So race around doesn't occur for the condition.

3. Option (D): When $CLK = 1$, $A = B = 0$

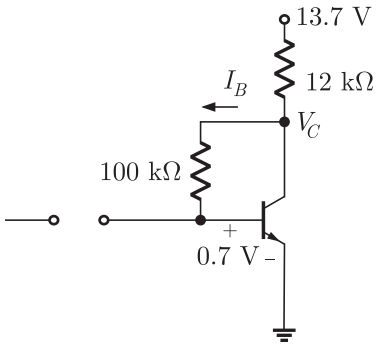
So, $A_1 = B_1 = 1$

And again as described for Option (B) race around doesn't occur for the condition.

So, Option (A) will be correct.

SOL 8.5 Option (D) is correct.

DC Analysis :



Using KVL in input loop,

$$V_C - 100I_B - 0.7 = 0$$

$$V_C = 100I_B + 0.7 \quad \text{...(i)}$$

$$I_C \simeq I_E = \frac{13.7 - V_C}{12k} = (\beta + 1)\, I_B$$

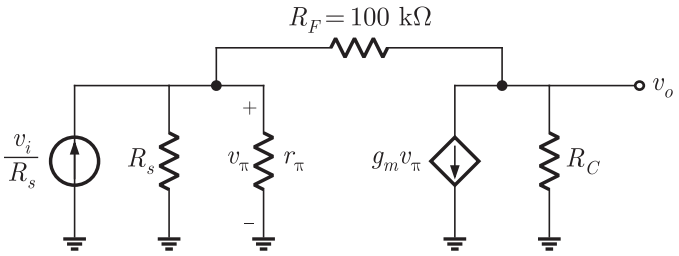
$$\frac{13.7 - V_C}{12 \times 10^3} = 100I_B \quad \text{...(ii)}$$

Solving equation (i) and (ii),

$$I_B = 0.01\,\text{mA}$$

Small Signal Analysis :

Transforming given input voltage source into equivalent current source.



This is a shunt-shunt feedback amplifier.

Given parameters,

$$r_\pi = \frac{V_T}{I_B} = \frac{25\,\text{mV}}{0.01\,\text{mA}} = 2.5\,\text{k}\Omega$$

$$g_m = \frac{\beta}{r_\pi} = \frac{100}{2.5 \times 1000} = 0.04\,\text{s}$$

Writing KCL at output node

$$\frac{v_0}{R_C} + g_m v_\pi + \frac{v_0 - v_\pi}{R_F} = 0$$

$$v_0\left[\frac{1}{R_C} + \frac{1}{R_F}\right] + v_\pi\left[g_m - \frac{1}{R_F}\right] = 0$$

Substituting $R_C = 12\,\text{k}\Omega,\ R_F = 100\,\text{k}\Omega,\ g_m = 0.04\,\text{s}$

$$v_0(9.33 \times 10^{-5}) + v_\pi(0.04) = 0$$

$$v_0 = -428.72\, V_\pi \quad \text{...(i)}$$

Writing KCL at input node

$$\frac{v_i}{R_s} = \frac{v_\pi}{R_s} + \frac{v_\pi}{r_\pi} + \frac{v_\pi - v_o}{R_F} = v_\pi\left[\frac{1}{R_s} + \frac{1}{r_\pi} + \frac{1}{R_F}\right] - \frac{v_0}{R_F}$$

$$= v_\pi(5.1 \times 10^{-4}) - \frac{v_0}{R_F}$$

Substituting V_π from equation (i)

$$\frac{v_i}{R_s} = \frac{-5.1 \times 10^{-4}}{428.72} v_0 - \frac{v_0}{R_F}$$

$$\frac{v_i}{10 \times 10^3} = -1.16 \times 10^{-6} v_0 - 1 \times 10^{-5} v_0 \quad R_s = 10\,\text{k}\Omega \text{ (source resistance)}$$

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$$\frac{v_i}{10 \times 10^3} = -1.116 \times 10^{-5}$$

$$|A_v| = \left|\frac{v_0}{v_i}\right| = \frac{1}{10 \times 10^3 \times 1.116 \times 10^{-5}} \simeq 8.96$$

SOL 8.6 Option (D) is correct.

Let Q_{n+1} is next state and Q_n is the present state. From the given below figure.

$$D = Y = \overline{A}X_0 + AX_1$$

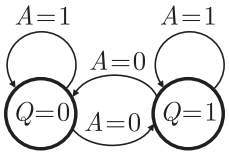
$$Q_{n+1} = D = \overline{A}X_0 + AX_1$$

$$Q_{n+1} = \overline{A}\,\overline{Q_n} + AQ_n \qquad X_0 = \overline{Q},\ X_1 = Q$$

If $A = 0$, $Q_{n+1} = \overline{Q_n}$ (toggle of previous state)

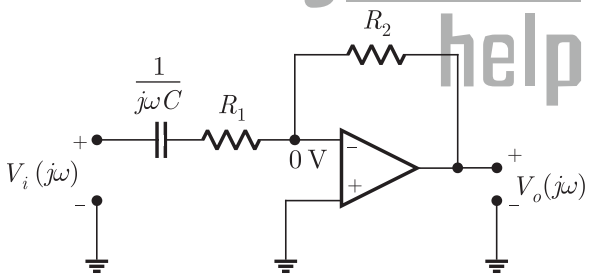
If $A = 1$, $Q_{n+1} = Q_n$

So state diagram is



SOL 8.7 Option (B) is correct.

First we obtain the transfer function.



$$\frac{0 - V_i(j\omega)}{\frac{1}{j\omega C} + R_1} + \frac{0 - V_o(j\omega)}{R_2} = 0$$

$$\frac{V_o(j\omega)}{R_2} = \frac{-V_i(j\omega)}{\frac{1}{j\omega C} + R_1}$$

$$V_o(j\omega) = -\frac{V_i(j\omega)\,R_2}{R_1 - j\frac{1}{\omega C}}$$

At $\omega \to 0$ (Low frequencies), $\frac{1}{\omega C} \to \infty$, so $V_o = 0$

At $\omega \to \infty$ (higher frequencies), $\frac{1}{\omega C} \to 0$, so $V_o(j\omega) = -\frac{R_2}{R_1}V_i(j\omega)$

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The filter passes high frequencies so it is a high pass filter.

$$H(j\omega) = \frac{V_o}{V_i} = \frac{-R_2}{R_1 - j\frac{1}{\omega C}}$$

$$\left|H(\infty)\right| = \left|\frac{-R_2}{R_1}\right| = \frac{R_2}{R_1}$$

At 3 dB frequency, gain will be $\sqrt{2}$ times of maximum gain $[H(\infty)]$

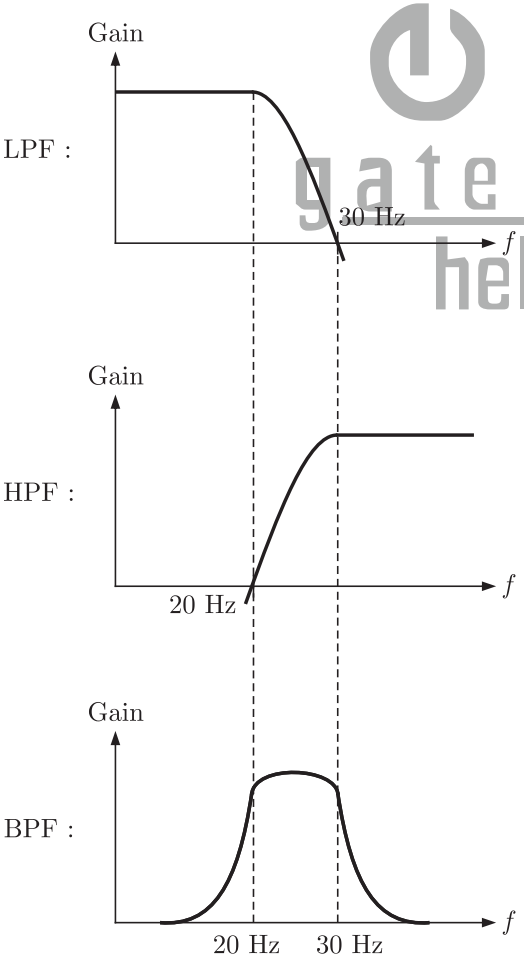
$$\left|H(j\omega_0)\right| = \frac{1}{\sqrt{2}}\left|H(\infty)\right|$$

So,
$$\frac{R_2}{\sqrt{R_1^2 + \frac{1}{\omega_0^2 C^2}}} = \frac{1}{\sqrt{2}}\left(\frac{R_2}{R_1}\right)$$

$$2R_1^2 = R_1^2 + \frac{1}{\omega_0^2 C^2} \Rightarrow R_1^2 = \frac{1}{\omega^2 C^2}$$

$$\omega_0 = \frac{1}{R_1 C}$$

SOL 8.8 Option (D) is correct.



So, it will act as a Band pass filter.

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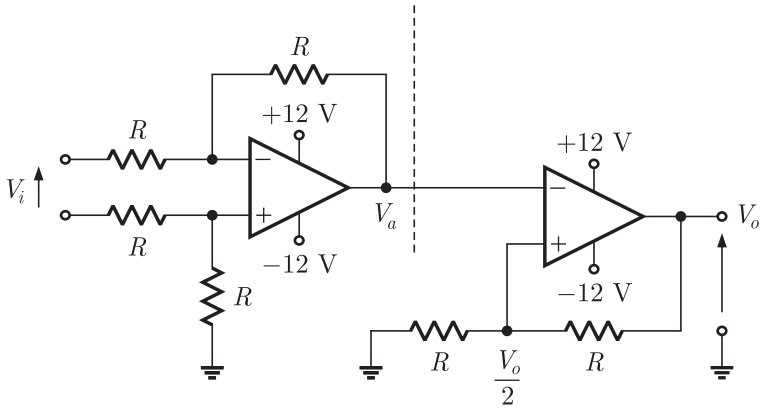
SOL 8.9 Option (D) is correct.



The first half of the circuit is a differential amplifier (negative feedback)

$$V_a = -(V_i)$$

Second op-amp has a positive feedback, so it acts as an schmitt trigger.

Since

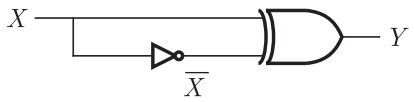
$$V_a = -V_i$$ this is a non-inverting schmitt trigger.

Threshold value

$$V_{TH} = \frac{12}{2} = 6\text{ V}$$

$$V_{TL} = -6\text{ V}$$

SOL 8.10 Option (A) is correct.



$$\begin{aligned} Y &= X \oplus \overline{X} \\ &= X\,\overline{\overline{X}} + \overline{X}X \\ &= XX + \overline{X}\,\overline{X} \\ &= X + \overline{X} = 1 \end{aligned}$$

SOL 8.11 Option (C) is correct.

LXI D, DISP
LP : CALL SUB
LP + 3

When CALL SUB is executed LP+3 value is pushed(inserted) in the stack.

POP H $\Rightarrow HL = LP + 3$

DAD D $\Rightarrow HL = HL + DE$

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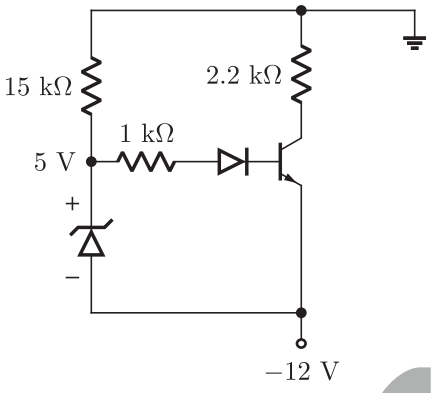
$= LP + 3 + DE$

PUSH H $\Rightarrow$ The last two value of the stack will be HL value i.e, $LP + DISP + 3$

SOL 8.12 Option (D) is correct.

Zener Diode is used as stabilizer.

The circuit is assumed to be as



We can see that both BE and BC Junction are forwarded biased. So the BJT is operating in saturation.

Collector current $I_C = \dfrac{12 - 0.2}{2.2k} = 5.36\,\text{mA}$

Note:- In saturation mode $I_C \neq \beta I_B$

SOL 8.13 Option (C) is correct.

The characteristics equation of the JK flip-flop is

$$Q_{n+1} = J\overline{Q}_n + \overline{K}Q_n$$

Q_{n+1} is the next state

From figure it is clear that

$$J = \overline{Q_B}\,; K = Q_B$$

The output of JK flip flop

$$Q_{A(n+1)} = \overline{Q_B}\,\overline{Q_A} + \overline{Q_B}\,Q_A = \overline{Q_B}(\overline{Q_A} + Q_A) = \overline{Q_B}$$

Output of T flip-flop

$$Q_{B(n+1)} = \overline{Q}_A$$

Clock pulse	Q_A	Q_B	$Q_{A(n+1)}$	$Q_{B(n+1)}$
Initially(t_n)	1	0	1	0
$t_n + 1$	1	0	1	0
$t_n + 2$	1	0	1	0
$t_n + 3$	1	0	1	0

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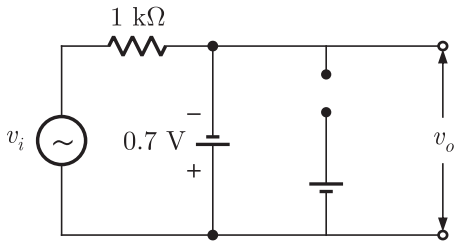
SOL 8.14 Option (C) is correct.

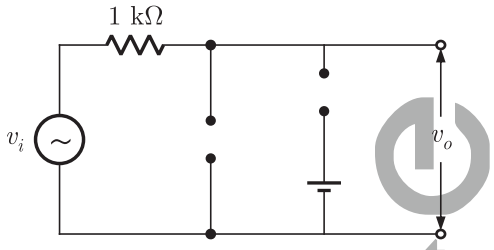
We can obtain three operating regions depending on whether the Zener and PN diodes are forward biased or reversed biased.

1. $v_i \leq -0.7\ \text{V}$, zener diode becomes forward biased and diode D will be off so the equivalent circuit looks like



The output $v_o = -0.7\ \text{V}$

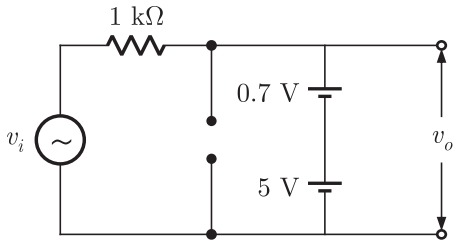
2. When $-0.7 < v_i \leq 5.7$, both zener and diode D will be off. The circuit is



Output follows input i.e $v_o = v_i$

Note that zener goes in reverse breakdown(i.e acts as a constant battery) only when difference between its p-n junction voltages exceeds 10 V.

3. When $v_i > 5.7\ \text{V}$, the diode D will be forward biased and zener remains off, the equivalent circuit is



$$v_o = 5 + 0.7 = 5.7\ \text{V}$$

SOL 8.15 Option (B) is correct.

Since the op-amp is ideal

$$v_+ = v_- = +2\ \text{volt}$$

By writing node equation

$$\frac{v_- - 0}{R} + \frac{v_- - v_o}{2R} = 0$$

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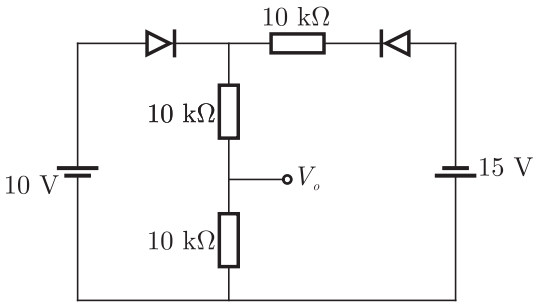
$$\frac{2}{R}+\frac{(2-v_o)}{2R}=0$$

$$4+2-v_o=0$$

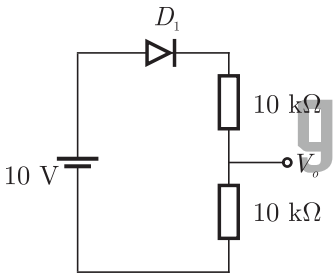
$$v_o=6 \text{ volt}$$

SOL 8.16 Option (B) is correct.

Given circuit is,



We can observe that diode D_2 is always off, whether D_1,is on or off. So equivalent circuit is.



D_1 is ON in this condition and

$$V_0=\frac{10}{10+10}\times 10$$

$$=5 \text{ volt}$$

SOL 8.17 Option (A) is correct.

By writing KVL equation for input loop (Base emitter loop)

$$10-(10\,\text{k}\Omega)\,I_B-V_{BE}-V_0=0 \qquad ...(1)$$

Emitter current $I_E=\dfrac{V_0}{100}$

$$I_C \simeq I_E=\beta I_B$$

So,

$$\frac{V_0}{100}=100I_B$$

$$I_B=\frac{V_0}{10\times 10^3}$$

Put I_B into equation (1)

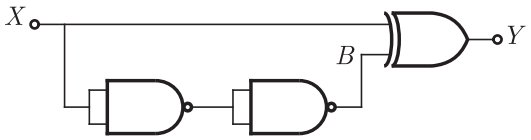
$$10 - (10 \times 10^3)\frac{V_0}{10 \times 10^3} - 0.7 - V_0 = 0$$

$$9.3 - 2V_0 = 0$$

$$\Rightarrow \quad V_0 = \frac{9.3}{2} = 4.65 \text{ A}$$

SOL 8.18 Option (A) is correct.

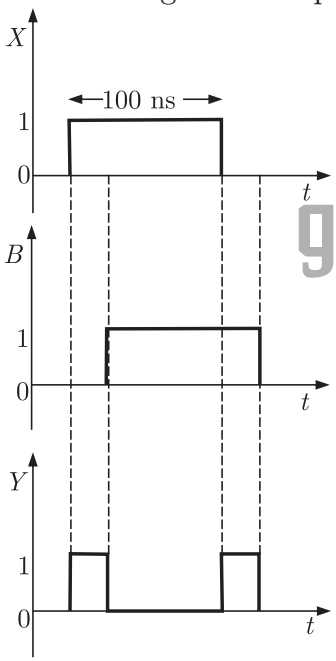
The circuit is



Output Y is written as

$$Y = X \oplus B$$

Since each gate has a propagation delay of 10 ns.



SOL 8.19 Option (D) is correct.

CALL, Address performs two operations

(1) PUSH PC $\Rightarrow$ Save the contents of PC (Program Counter) into stack.

$$\text{SP} = \text{SP} - 2 \text{ (decrement)}$$

$$((\text{SP})) \leftarrow (\text{PC})$$

(2) Addr stored in PC.

$$(\text{PC}) \leftarrow \text{Addr}$$

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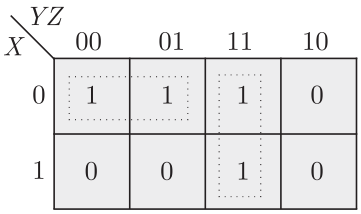
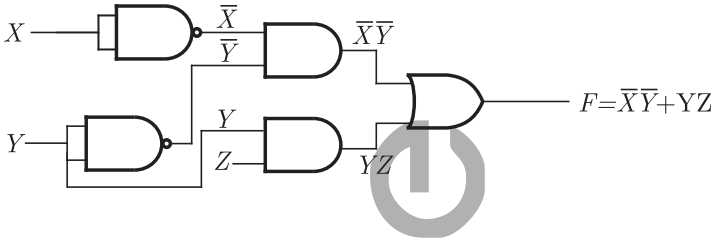
SOL 8.20 Option (B) is correct.
Function F can be minimized by grouping of all 1's in K-map as following.



$$F = \overline{X}\,\overline{Y} + YZ$$

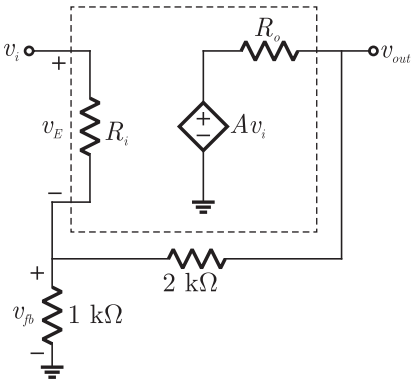
SOL 8.21 Option (D) is correct.
Since $F = \overline{X}\,\overline{Y} + YZ$
In option (D)



SOL 8.22 Option (A) is correct.
Figure shows current characteristic of diode during switching.

SOL 8.23 Option (B) is correct.
The increasing order of speed is as following
Magnetic tape> CD-ROM> Dynamic RAM>Cache Memory>Processor register

SOL 8.24 Option (B) is correct.
Equivalent circuit of given amplifier



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Feedback samples output voltage and adds a negative feedback voltage (v_{fb}) to input.
So, it is a voltage-voltage feedback.

SOL 8.25 Option () is correct.
NOR and NAND gates considered as universal gates.

SOL 8.26 Option (A) is correct.
Let voltages at positive and negative terminals of op-amp are V_+ and V_- respectively, then

$$V_+ = V_- = V_s \text{ (ideal op-amp)}$$

In the circuit we have,

$$\frac{V_- - 0}{\left(\frac{1}{Cs}\right)} + \frac{V_- - V_0(s)}{R} = 0$$

$$(RCs)\, V_- + V_- - V_0(s) = 0$$

$$(1 + RCs)\, V_s = V_0(s)$$

Similarly current I_s is, $I_s = \dfrac{V_s - V_0}{R}$

$$I_s = \frac{RCs}{R} V_s$$

$$I_s = j\omega C V_s$$

$$I_s = |\omega C V_s| \angle + 90^\circ$$

$$|I_s| = 2\pi f \times 10 \times 10^{-6} \times 10$$

$$|I_s| = 2 \times \pi \times 50 \times 10 \times 10^{-6} \times 10$$

$$|I_s| = 10\pi \text{ mA, leading by } 90^\circ$$

SOL 8.27 Option (D) is correct.
Input and output power of a transformer is same

$$P_{in} = P_{out}$$

for emitter follower, voltage gain $(A_v) = 1$

current gain $(A_i) > 1$

Power $(P_{out}) = A_v A_i P_{in}$

Since emitter follower has a high current gain so $P_{out} > P_{in}$

SOL 8.28 Option (D) is correct.
For the given instruction set,

XRA $A \Rightarrow$ XOR A with $A \Rightarrow$ A = 0

MVI B, F0 H $\Rightarrow B$ = F0 H

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$$\begin{aligned}\text{SUB } B \Rightarrow A &= A - B\\ A &= 00000000\\ B &= 11110000\\ \text{2's complement of } (-B) &= \underline{00010000}\\ A + (-B) = A - B &= 00010000\\ &= 10\,\text{H}\end{aligned}$$

SOL 8.29 Option (D) is correct.

This is a schmitt trigger circuit, output can takes two states only.

$$V_{OH} = +6 \text{ volt}$$
$$V_{OL} = -3 \text{ volt}$$

Threshold voltages at non-inverting terminals of op-amp is given as

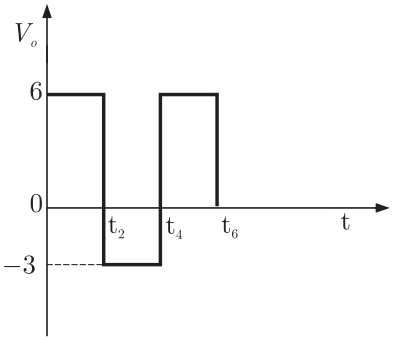
$$\frac{V_{TH} - 6}{2} + \frac{V_{TH} - 0}{1} = 0$$
$$3V_{TH} - 6 = 0$$
$$V_{TH} = 2 \text{ V} \quad \text{(Upper threshold)}$$

Similarly

$$\frac{V_{TL} - (-3)}{2} + \frac{V_{TL}}{1} = 0$$
$$3V_{TL} + 3 = 0$$
$$V_{TL} = -1 \text{ V} \quad \text{(Lower threshold)}$$

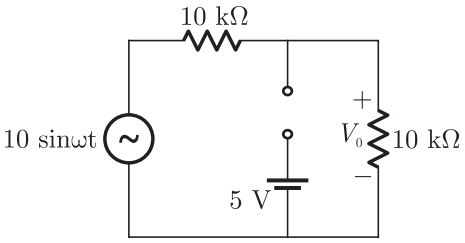
For
$$V_{in} < 2 \text{ Volt}, \; V_0 = +6 \text{ Volt}$$
$$V_{in} > 2 \text{ Volt}, \; V_0 = -3 \text{ Volt}$$
$$V_{in} < -1 \text{ Volt} \; V_0 = +6 \text{ Volt}$$
$$V_{in} > -1 \text{ Volt} \; V_0 = -3 \text{ Volt}$$

Output waveform



SOL 8.30 Option (A) is correct.

Assume the diode is in reverse bias so equivalent circuit is

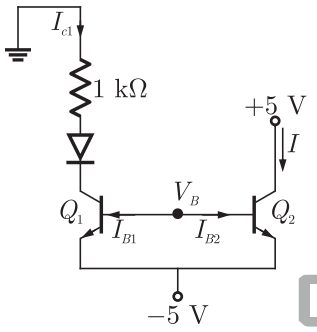


Output voltage $V_0 = \dfrac{10\sin\omega t}{10+10} \times 10 = 5\sin\omega t$

Due to resistor divider, voltage across diode $V_D < 0$ (always). So it in reverse bias for given input.

Output, $V_0 = 5\sin\omega t$

SOL 8.31 Option (C) is correct.



This is a current mirror circuit. Since β is high so $I_{C1} = I_{C2}, I_{B1} = I_{B2}$

$$V_B = (-5 + 0.7)$$
$$= -4.3 \text{ volt}$$

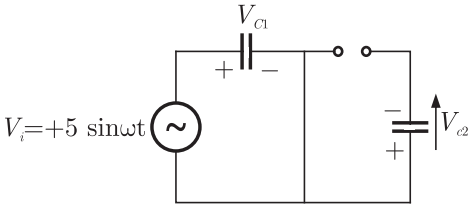
Diode D_1 is forward biased.

So, current I is, $I = I_{C2} = I_{C1}$

$$= \frac{0-(-4.3)}{1} = 4.3 \text{ mA}$$

SOL 8.32 Option (D) is correct.

In positive half cycle of input, diode D_1 is in forward bias and D_2 is off, the equivalent circuit is



Capacitor C_1 will charge upto +5 volt. $V_{C1} = +5$ volt

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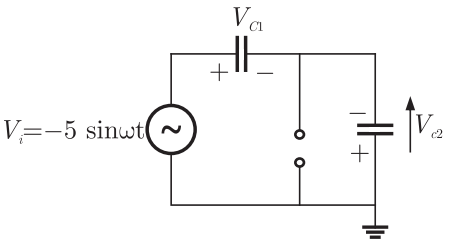
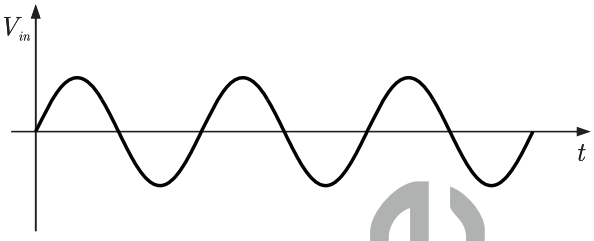
In negative halt cycle diode D_1 is off and D_2 is on.



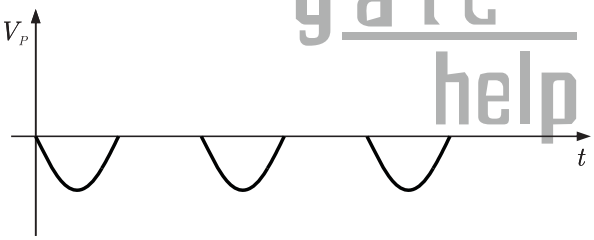
Now capacitor V_{C2} will charge upto -10 volt in opposite direction.

SOL 8.33 Option () is correct.

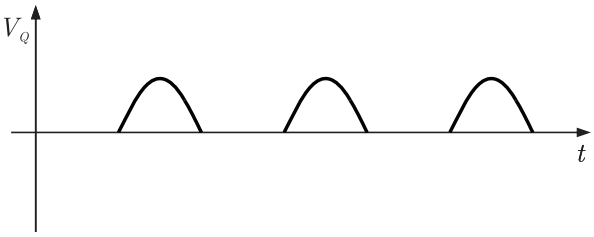
Let input V_{in} is a sine wave shown below



According to given transfer characteristics of rectifiers output of rectifier P is.



Similarly output of rectifier Q is



Output of a full wave rectifier is given as

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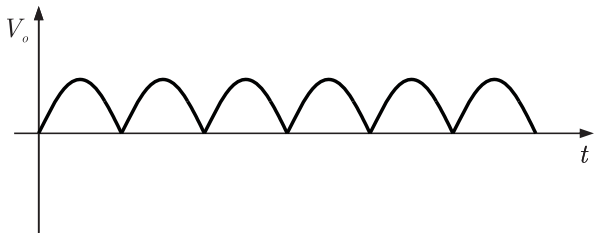


To get output V_0

$$V_0 = \mathrm{K}(-V_P + V_Q) \qquad \mathrm{K} - \text{gain of op-amp}$$

So, P should connected at inverting terminal of op-amp and Q with non-inverting terminal.

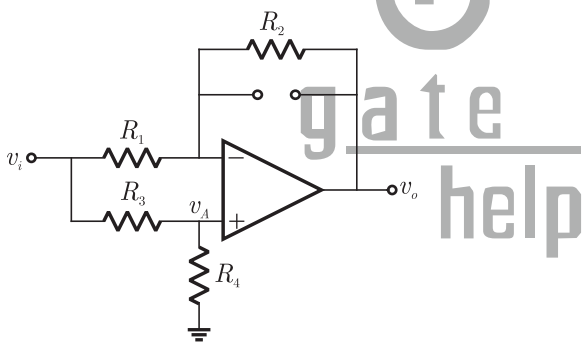
SOL 8.34 Option () is correct.

SOL 8.35 Option (C) is correct.

For low frequencies,

$\omega \to 0$, so $\dfrac{1}{\omega C} \to \infty$

Equivalent circuit is,



Applying node equation at positive and negative input terminals of op-amp.

$$\frac{v_A - v_i}{R_1} + \frac{v_A - v_o}{R_2} = 0$$

$$2v_A = v_i + v_o, \qquad \because\ R_1 = R_2 = R_A$$

Similarly,

$$\frac{v_A - v_i}{R_3} + \frac{v_A - 0}{R_4} = 0$$

$$2v_A = v_{in}, \qquad \because\ R_3 = R_4 = R_B$$

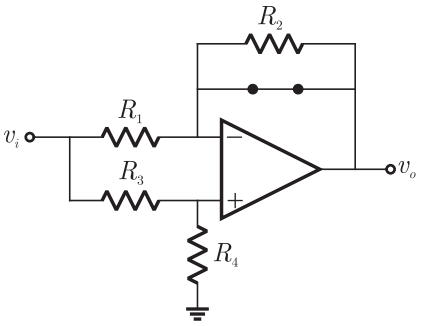
So, $v_o = 0$

It will stop low frequency signals.

For high frequencies,

$\omega \to \infty$, then $\dfrac{1}{\omega C} \to 0$

Equivalent circuit is,



Output, $v_o = v_i$

So it will pass high frequency signal.

This is a high pass filter.

SOL 8.36 Option (D) is correct.

In Q.7.21 cutoff frequency of high pass filter is given by,

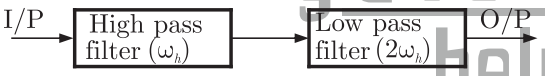
$$\omega_h = \frac{1}{2\pi R_A C}$$

Here given circuit is a low pass filter with cutoff frequency,

$$\omega_L = \frac{1}{2\pi \frac{R_A}{2} C} = \frac{2}{2\pi R_A C}$$

$$\omega_L = 2\omega_h$$

When both the circuits are connected together, equivalent circuit is,



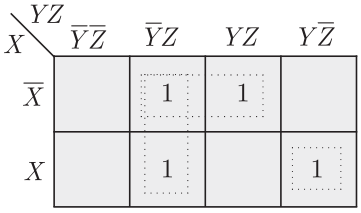
So this is is Band pass filter, amplitude response is given by.

SOL 8.37 Option (B) is correct.

In SOP form, F is written as

$$F = \Sigma m(1,3,5,6)$$
$$= \overline{X}\,\overline{Y}Z + \overline{X}\,Y\overline{Z} + X\overline{Y}Z + XY\overline{Z}$$

Solving from K- map



$$F = \overline{X}Z + \overline{Y}Z + XY\overline{Z}$$

In POS form $F = (Y+Z)(X+Z)(\overline{X}+\overline{Y}+\overline{Z})$

Since all outputs are active low so each input in above expression is complemented

$$F = (\overline{Y}+\overline{Z})(\overline{X}+\overline{Z})(X+Y+Z)$$

SOL 8.38 Option (B) is correct.

Given that $\text{SP} = 2700\,\text{H}$

$\text{PC} = 2100\,\text{H}$

$\text{HL} = 0000\,\text{H}$

Executing given instruction set in following steps,

DAD SP ⇒ Add register pair (SP) to HL register

$\text{HL} = \text{HL} + \text{SP}$

$\text{HL} = 0000\,\text{H} + 2700\,\text{H}$

$\text{HL} = 2700\,\text{H}$

PCHL ⇒ Load program counter with HL contents

$\text{PC} = \text{HL} = 2700\ \text{H}$

So after execution contents are,

$\text{PC} = 2700\ \text{H}, \text{HL} = 2700\ \text{H}$

SOL 8.39 Option (D) is correct.

If transistor is in normal active region, base current can be calculated as following,

By applying KVL for input loop,

$$10 - I_C(1\times10^3) - 0.7 - 270\times10^3 I_B = 0$$

$$\beta I_B + 270\, I_B = 9.3\ \text{mA}, \qquad \therefore I_C = \beta I_B$$

$$I_B(\beta + 270) = 9.3\ \text{mA}$$

$$I_B = \frac{9.3\,\text{mA}}{270+100} = 0.025\ \ \text{mA}$$

In saturation, base current is given by,

$$10 - I_C(1) - V_{CE} - I_E(1) = 0$$

$$\frac{10}{2} = I_{C\,(\text{sat})} \qquad I_C \simeq I_E,\ V_{CE} \simeq 0$$

$$I_{C\,(\text{sat})} = 5\ \text{mA}$$

$$I_{B(\text{sat})} = \frac{I_{C\,(\text{sat})}}{\beta} = \frac{5}{100} = .050\ \text{mA}$$

$I_B < I_{B(\text{sat})}$, so transistor is in forward active region.

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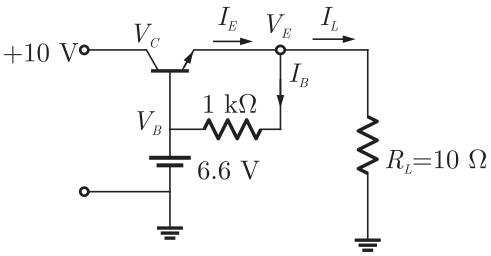
SOL 8.40 Option (B) is correct.

In the circuit



We can analyze that the transistor is operating in active region.

$$V_{BE(ON)} = 0.6 \text{ volt}$$
$$V_B - V_E = 0.6$$
$$6.6 - V_E = 0.6$$
$$V_E = 6.6 - 0.6 = 6 \text{ volt}$$

At emitter (by applying KCL),

$$I_E = I_B + I_L$$
$$I_E = \frac{6 - 6.6}{1\,\text{k}\Omega} + \frac{6}{10\,\Omega} \simeq 0.6\,\text{amp}$$

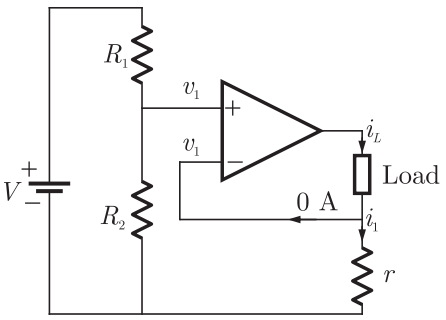
$V_{CE} = V_C - V_E = 10 - 6 = 4$ volt

Power dissipated in transistor is given by.

$$P_T = V_{CE} \times I_C = 4 \times 0.6 \qquad \therefore I_C \simeq I_E = 0.6 \text{ amp}$$
$$= 2.4 \text{ W}$$

SOL 8.41 Option (D) is correct.

This is a voltage-to-current converter circuit. Output current depends on input voltage.



Since op-amp is ideal $v_+ = v_- = v_1$

Writing node equation.

$$\frac{v_1 - v}{R_1} + \frac{v_1 - 0}{R_2} = 0$$

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$$v_1\left(\frac{R_1+R_2}{R_1R_2}\right)=\frac{V}{R_1}$$

$$v_1 = V\left(\frac{R_2}{R_1+R_2}\right)$$

Since the op-amp is ideal therefore

$$i_L = i_1 = \frac{v_1}{r} = \frac{V}{r}\left(\frac{R_2}{R_1+R_2}\right)$$

SOL 8.42 Option (D) is correct.

In the circuit output Y is given as

$$Y = [A \oplus B] \oplus [C \oplus D]$$

Output Y will be 1 if no. of 1's in the input is odd.

SOL 8.43 Option () is correct.

This is a class-B amplifier whose efficiency is given as

$$\eta = \frac{\pi}{4}\frac{V_P}{V_{CC}}$$

where $V_P \rightarrow$ peak value of input signal

$V_{CC} \rightarrow$ supply voltage

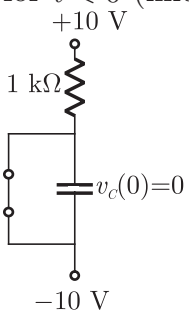
here $V_P = 7$ volt, $V_{CC} = 10$ volt

so, $$\eta = \frac{\pi}{4} \times \frac{7}{10} \times 100 = 54.95\% \simeq 55\%$$

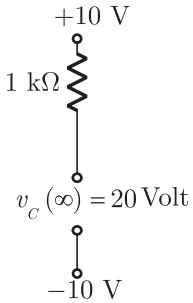
SOL 8.44 Option (B) is correct.

In the circuit the capacitor starts charging from 0 V (as switch was initially closed) towards a steady state value of 20 V.

for $t < 0$ (initial)



for $t \rightarrow \infty$ (steady state)



So at any time t, voltage across capacitor (i.e. at inverting terminal of op-amp) is given by

$$v_c(t) = v_c(\infty) + [v_c(0) - v_c(\infty)]\, e^{\frac{-t}{RC}}$$

$$v_c(t) = 20\,(1 - e^{\frac{-t}{RC}})$$

Voltage at positive terminal of op-amp

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$$\frac{v_+ - v_{out}}{10} + \frac{v_+ - 0}{100} = 0$$

$$v_+ = \frac{10}{11} v_{out}$$

Due to zener diodes, $-5 \le v_{out} \le +5$

So, $$v_+ = \frac{10}{11}(5) \text{ V}$$

Transistor form -5 V to $+5$ V occurs when capacitor charges upto v_+.

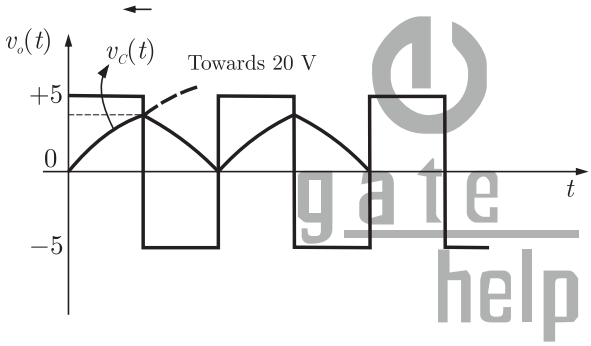
So $$20(1 - e^{-t/RC}) = \frac{10 \times 5}{11}$$

$$1 - e^{-t/RC} = \frac{5}{22}$$

$$\frac{17}{22} = e^{-t/RC}$$

$$t = RC \ln\left(\frac{22}{17}\right) = 1 \times 10^3 \times .01 \times 10^{-6} \times 0.257 = 2.57 \,\mu\text{sec}$$

Voltage waveforms in the circuit is shown below



SOL 8.45 Option (B) is correct.

First convert the given number from hexadecimal to its binary equivalent, then binary to octal.

Hexadecimal no. AB. CD

Binary equivalent $\underbrace{1010}_{A}\ \underbrace{1011}_{B} \cdot \underbrace{1100}_{C}\ \underbrace{1101}_{D}$

To convert in octal group three binary digits together as shown

$$\underbrace{010}_{2}\ \underbrace{101}_{5}\ \underbrace{011}_{3} \cdot \underbrace{110}_{6}\ \underbrace{011}_{3}\ \underbrace{010}_{2}$$

So, $$(AB.CD)_{\text{H}} = (253.632)_8$$

SOL 8.46 Option (B) is correct.

In a 555 astable multi vibrator circuit, charging of capacitor occurs through resistor $(R_A + R_B)$ and discharging through resistor R_B only. Time for charging and discharging is given as.

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$$T_C = 0.693(R_A + R_B)\,C = 0.693\,R_B\,C$$

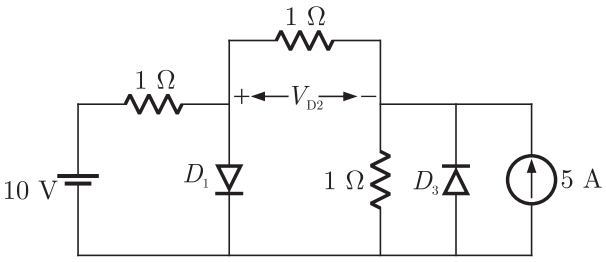
But in the given circuit the diode will go in the forward bias during charging, so the capacitor will charge through resistor R_A only and discharge through R_B only.

$\because$ $R_A = R_B$

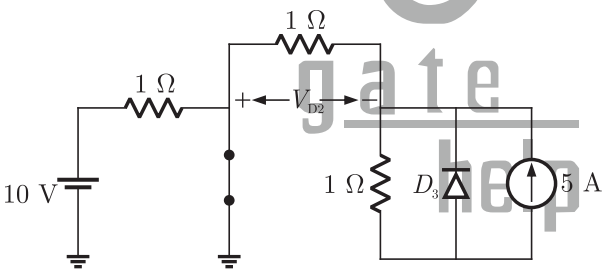
So $T_C = T_D$

SOL 8.47 Option (A) is correct.

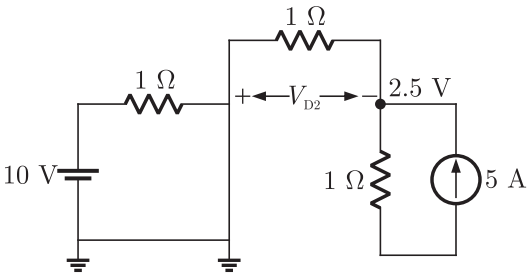
First we can check for diode D_2. Let diode D_2 is OFF then the circuit is



In the above circuit diode D_1 must be ON, as it is connected with 10 V battery now the circuit is



Because we assumed diode D_2 OFF so voltage across it $V_{D2} \leq 0$ and it is possible only when D_3 is off.



So, all assumptions are true.

SOL 8.48 Option (D) is correct.

In the positive half cycle of input, Diode D_1 will be reverse biased and equivalent circuit is.

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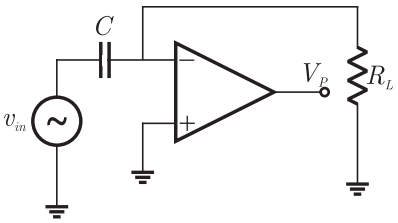
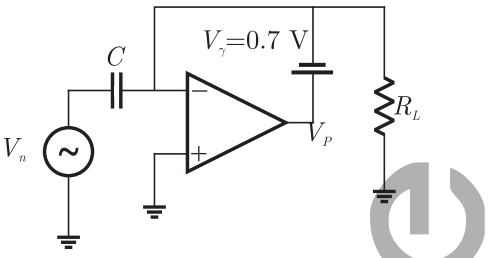


Since there is no feed back to the op-amp and op-amp has a high open loop gain so it goes in saturation. Input is applied at inverting terminal so.

$$V_P = -V_{CC} = -12 \text{ V}$$

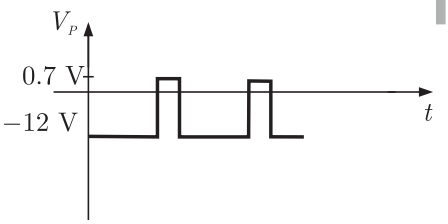
In negative half cycle of input, diode D_1 is in forward bias and equivalent circuit is shown below.



Output $V_P = V_\gamma + V_-$

Op-amp is at virtual ground so $V_+ = V_- = 0$ and $V_P = V_\gamma = 0.7$ V

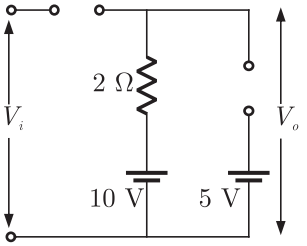
Voltage wave form at point P is



SOL 8.49 Option (A) is correct.

In the circuit when $V_i < 10$ V, both D_1 and D_2 are off.

So equivalent circuit is,



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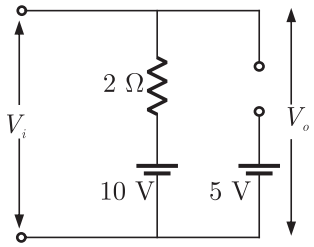
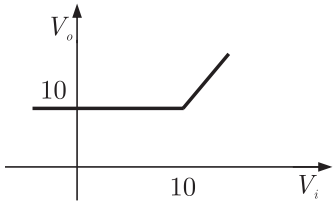
Output, $V_o = 10$ volt

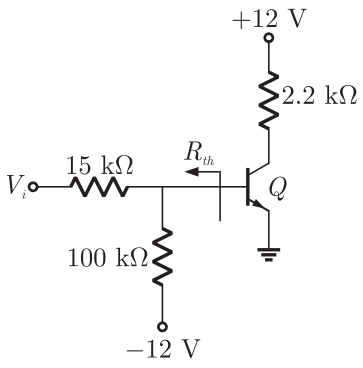
When $V_i > 10$ V (D_1 is in forward bias and D_2 is off
So the equivalent circuit is,



Output, $V_o = V_i$
Transfer characteristic of the circuit is



SOL 8.50 Option (B) is correct.
Assume that BJT is in active region, thevenin equivalent of input circuit is obtained as



$$\frac{V_{th} - V_i}{15} + \frac{V_{th} - (-12)}{100} = 0$$

$$20\,V_{th} - 20\,V_i + 3\,V_{th} + 36 = 0$$

$$23\,V_{th} = 20 \times 5 - 36,\ V_i = 5 \text{ V}$$

$$V_{th} = 2.78 \text{ V}$$

Thevenin resistance $R_{th} = 15\,\text{K}\Omega \,||\, 100\,\text{K}\Omega$

$$= 13.04\,\text{K}\Omega$$

So the circuit is

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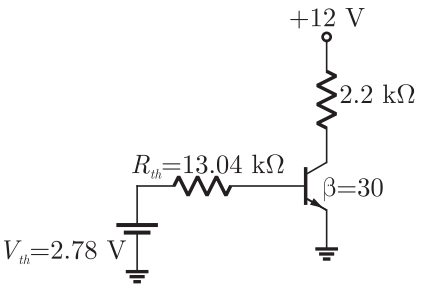


Writing KVL for input loop

$$2.78 - R_{th} I_B - 0.7 = 0$$

$$I_B = 0.157 \text{ mA}$$

Current in saturation is given as,

$$I_{B(\text{sat})} = \frac{I_{C(\text{sat})}}{\beta}$$

$$I_{C(\text{sat})} = \frac{12.2}{2.2} = 5.4 \text{ mA}$$

So,
$$I_{B(\text{sat})} = \frac{5.45 \text{ mA}}{30} = 0.181 \text{ mA}$$

Since $I_{B(\text{sat})} > I_B$, therefore assumption is true.

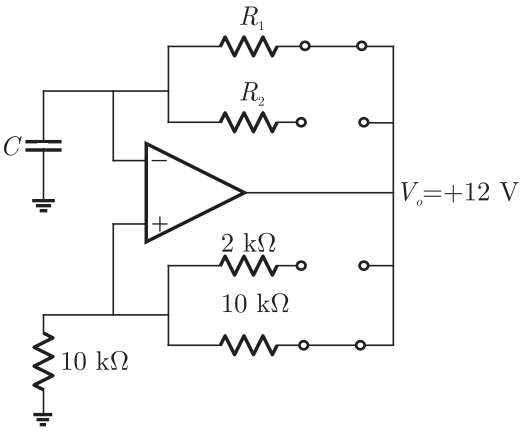
SOL 8.51 Option (C) is correct.

Here output of the multi vibrator is

$$V_0 = \pm 12 \text{ volt}$$

Threshold voltage at positive terminal of op-amp can be obtained as following

When output $V_0 = +12$ V, equivalent circuit is,



writing node equation at positive terminal of op-amp

$$\frac{V_{th} - 12}{10} + \frac{V_{th} - 0}{10} = 0$$

$$V_{th} = 6 \text{ volt} \quad \text{(Positive threshold)}$$

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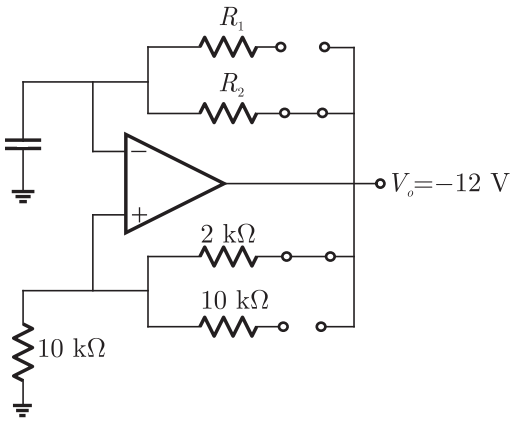
So, the capacitor will charge upto 6 volt.
When output $V_0 = -12$ V, the equivalent circuit is.



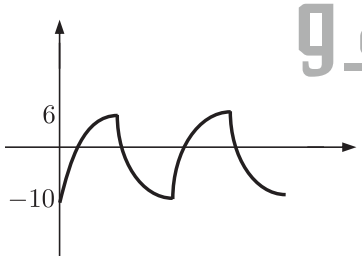
node equation

$$\frac{V_{th}+12}{2}+\frac{V_{th}-0}{10}=0$$

$$5\,V_{th}+60+V_{th}=0$$

$$V_{th}=-10 \text{ volt} \quad \text{(negative threshold)}$$

So the capacitor will discharge upto -10 volt.
At terminal P voltage waveform is.



SOL 8.52 Option () is correct.

SOL 8.53 Option () is correct.

SOL 8.54 Option (A) is correct.
Function F can be obtain as,

$$\begin{aligned}F &= I_0\overline{S}_1\overline{S}_0+I_1\overline{S}_1S_0+I_2S_1\overline{S}_0+I_3S_1S_0\\ &= A\overline{B}\,\overline{C}+\overline{A}\,\overline{B}\,C+1\cdot B\overline{C}+0\cdot BC\\ &= A\overline{B}\,\overline{C}+\overline{A}\,\overline{B}C+B\overline{C}\;=A\overline{B}\,\overline{C}+\overline{A}\,\overline{B}C+B\overline{C}(A+\overline{A})\\ &= A\overline{B}\,\overline{C}+\overline{A}\,\overline{B}C+AB\overline{C}+\overline{A}\,B\overline{C}\\ &= \Sigma(1,2,4,6)\end{aligned}$$

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SOL 8.55 Option (A) is correct.

MVI H and MVI L stores the value 255 in H and L registers. DCR L decrements L by 1 and JNZ checks whether the value of L is zero or not. So DCR L executed 255 times till value of L becomes '0'.

Then DCR H will be executed and it goes to 'Loop' again, since L is of 8 bit so no more decrement possible and it terminates.

SOL 8.56 Option (A) is correct.

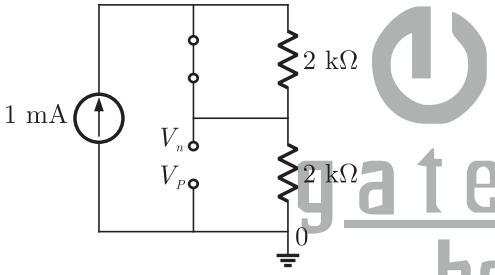
XCHG⇒ Exchange the contain of DE register pair with HL pair So now addresses of memory locations are stored in HL pair.

INR M⇒ Increment the contents of memory whose address is stored in HL pair.

SOL 8.57 Option (A) is correct.

From the circuit we can observe that Diode D_1 must be in forward bias (since current is flowing through diode).

Let assume that D_2 is in reverse bias, so equivalent circuit is.



Voltage V_n is given by

$$V_n = 1 \times 2 = 2 \text{ Volt}$$

$$V_p = 0$$

$V_n > V_p$ (so diode is in reverse bias, assumption is true)

Current through D_2 is $I_{D2} = 0$

SOL 8.58 Option (C) is correct.

SHLD transfers contain of HL pair to memory location.

SHLD 2050 ⇒ L → M [2050H]

H → M [2051H]

SOL 8.59 Option (D) is correct.

This is a N-channel MOSFET with $V_{GS} = 2$ V

$$V_{TH} = +1 \text{ V}$$

$$V_{DS(\text{sat})} = V_{GS} - V_{TH}$$

$$V_{DS(\text{sat})} = 2 - 1 = 1 \text{ V}$$

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Due to 10 V source $V_{DS} > V_{DS(\text{sat})}$ so the NMOS goes in saturation, channel conductivity is high and a high current flows through drain to source and it acts as a short circuit.

So, $V_{ab} = 0$

SOL 8.60 Option (C) is correct.

Let the present state is Q(t), so input to D-flip flop is given by,

$$D = Q(t) \oplus X$$

Next state can be obtained as,

$$\begin{aligned} Q(t+1) &= D \\ &= Q(t) \oplus X \\ &= Q(t)\,\overline{X} + \overline{Q}(t)\,X \\ &= \overline{Q}(t), \quad \text{if } X = 1 \end{aligned}$$

and $Q(t+1) = Q(t), \quad \text{if } X = 0$

So the circuit behaves as a T flip flop.

SOL 8.61 Option (B) is correct.

Since the transistor is operating in active region.

$$I_E \approx \beta I_B$$

$$I_B = \frac{I_E}{\beta} = \frac{1\text{ mA}}{100} = 10\ \mu\text{A}$$

SOL 8.62 Option (C) is correct.

Gain of the inverting amplifier is given by,

$$A_v = -\frac{R_F}{R_1} = -\frac{1\times 10^6}{R_1}, \qquad R_F = 1 \ \ \text{M}\Omega$$

$$R_1 = -\frac{1\times 10^6}{A_v}$$

$A_v = -10$ to -25 so value of R_1

$$R_1 = \frac{10^6}{10} = 100\ \text{k}\Omega \qquad \text{for } A_v = -10$$

$$R_1' = \frac{10^6}{25} = 40\ \text{k}\Omega \qquad \text{for } A_v = -25$$

R_1 should be as large as possible so $R_1 = 100\ \text{k}\Omega$

SOL 8.63 Option (B) is correct.

Direct coupled amplifiers or DC-coupled amplifiers provides gain at dc or very low frequency also.

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SOL 8.64 Option (C) is correct.

Since there is no feedback in the circuit and ideally op-amp has a very high value of open loop gain, so it goes into saturation (ouput is either $+V$ or $-V$) for small values of input.

The input is applied to negative terminal of op-amp, so in positive half cycle it saturates to $-V$ and in negative half cycle it goes to $+V$.

SOL 8.65 Option (B) is correct.

CHECK From the given input output waveforms truth table for the circuit is drawn as

X_1	X_2	Q
1	0	1
0	0	1
0	1	0

In option (A), for $X_1 = 1, Q = 0$ so it is eliminated.

In option (C), for $X_1 = 0, Q = 0$ (always), so it is also eliminated.

In option (D), for $X_1 = 0, Q = 1$, which does not match the truth table.

Only option (B) satisfies the truth table.

SOL 8.66 Option (D) is correct.

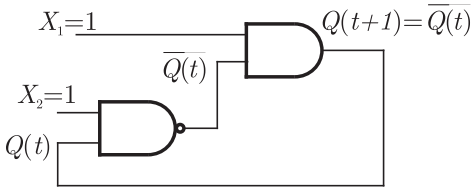
In the given circuit NMOS Q_1 and Q_3 makes an inverter circuit. Q_4 and Q_5 are in parallel works as an OR circuit and Q_2 is an output inverter.

So output is

$$Q = \overline{\overline{X_1} + X_2} = X_1.\overline{X_2}$$

SOL 8.67 Option (D) is correct.

Let $Q(t)$ is the present state then from the circuit,



So, the next state is given by

$$Q(t+1) = \overline{Q}(t) \text{ (unstable)}$$

SOL 8.68 Option (B) is correct.

Trans-conductance of MOSFET is given by

$$g_m = \frac{\partial i_D}{\partial V_{GS}}$$

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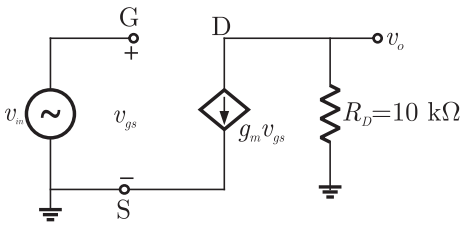
$$= \frac{(2-1)\text{ mA}}{(2-1)\text{ V}} = 1\text{ mS}$$

SOL 8.69 Option (D) is correct.

Voltage gain can be obtain by small signal equivalent circuit of given amplifier.



$$v_o = -\, g_m\, v_{gs}\, R_D$$

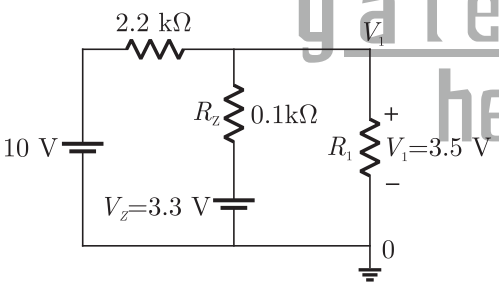
$$v_{gs} = v_{in}$$

So, $$v_o = -\, g_m\, R_D\, v_{in}$$

Voltage gain $$A_v = \frac{v_o}{v_i} = -\, g_m R_D = -\,(1\text{ mS})\,(10\text{ k}\Omega) = -\,10$$

SOL 8.70 Option (C) is correct.

Given circuit,



In the circuit

$$V_1 = 3.5\text{ V (given)}$$

Current in zener is.

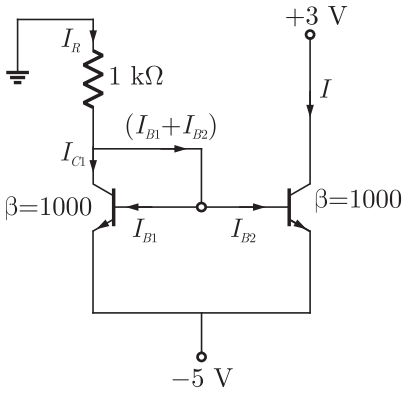
$$I_Z = \frac{V_1 - V_Z}{R_Z} = \frac{3.5 - 3.3}{0.1 \times 10^3} = 2\text{ mA}$$

SOL 8.71 Option (C) is correct.

This is a current mirror circuit. Since V_{BE} is the same in both devices, and transistors are perfectly matched, then

$$I_{B1} = I_{B2} \quad \text{and} \quad I_{C1} = I_{C2}$$

From the circuit we have,



$$I_R = I_{C1} + I_{B1} + I_{B2} = I_{C1} + 2I_{B2} \qquad \because I_{B1} = I_{B2}$$

$$= I_{C2} + \frac{2I_{C2}}{\beta} \qquad \because I_{C1} = I_{C2}, I_{C2} = \beta I_{B2}$$

$$I_R = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C2} = I = \frac{I_R}{\left(1 + \frac{2}{\beta}\right)}$$

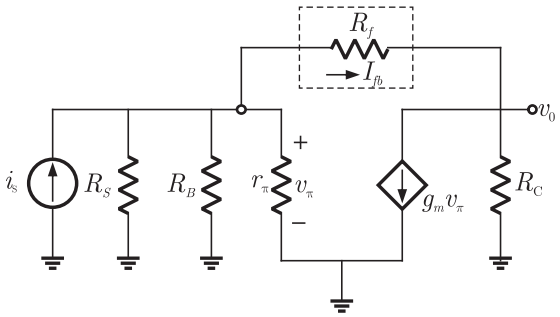
I_R can be calculate as

$$I_R = \frac{-5 + 0.7}{1 \times 10^3} = -4.3 \text{ mA}$$

So,
$$I = \frac{4.3}{\left(1 + \frac{2}{100}\right)} \simeq 4.3 \text{ mA}$$

SOL 8.72 Option (B) is correct.

The small signal equivalent circuit of given amplifier



Here the feedback circuit samples the output voltage and produces a feed back current I_{fb} which is in shunt with input signal. So this is a shunt-shunt feedback configuration.

SOL 8.73 Option (A) is correct.

In the given circuit output is stable for both 1 or 0. So it is a bistable multivibrator.

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SOL 8.74 Option (A) is correct.

Since there are two levels ($+ V_{CC}$ *or* $- V_{CC}$) of output in the given comparator circuit.

For an n-bit Quantizer

$$2^n = \text{No. of levels}$$
$$2^n = 2$$
$$n = 1$$

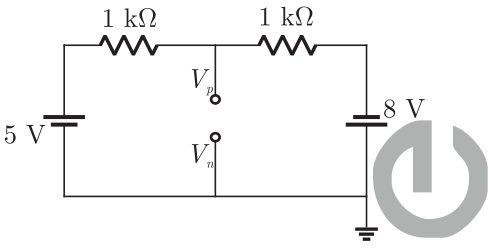
SOL 8.75 Option (C) is correct.

From the circuit, we can see the that diode D_2 must be in forward Bias.

For D_1 let assume it is in reverse bias.

Voltages at p and n terminal of D_1 is given by V_p and V_n

$V_p < V_n$ (D_1 is reverse biased)



Applying node equation

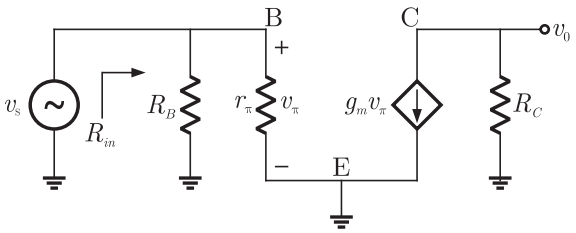
$$\frac{V_p - 5}{1} + \frac{V_p + 8}{1} = 0$$
$$2V_p = -3$$
$$V_p = -1.5$$
$$V_n = 0$$

$V_p < V_n$ (so the assumption is true and D_1 is in reverse bias) and current in D_1

$$I_{D1} = 0 \text{ mA}$$

SOL 8.76 Option (D) is correct.

The small signal ac equivalent circuit of given amplifier is as following.



Here $R_B = (10 \text{ k}\Omega \parallel 10 \text{ k}\Omega) = 5 \text{ k}\Omega$

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$$g_m = 10\,\text{ms}$$

$$\because\ g_m r_\pi = \beta \Rightarrow r_\pi = \frac{50}{10\times 10^{-3}} = 5\,\text{k}\Omega$$

Input resistance

$$R_{in} = R_B \parallel r_\pi = 5\ \text{k}\Omega \parallel 5\ \text{k}\Omega = 2.5\,\text{k}\Omega$$

SOL 8.77 Option (D) is correct.

For PMOS to be biased in non-saturation region.

$$V_{SD} < V_{SD(\text{sat})}$$

and

$$V_{SD(\text{sat})} = V_{SG} + V_T$$

$$V_{SD(\text{sat})} = 4 - 1 \qquad \{\because\ V_{SG} = 4 - 0 = 4\ \text{volt}$$

$$= 3\,\text{Volt}$$

So, $V_{SD} < 3$

$$V_S - V_D < 3$$

$$4 - I_D R < 3$$

$$1 < I_D R$$

$$I_D R > 1, \qquad I_D = 1\ \text{mA}$$

$$R > 1000\ \Omega$$

SOL 8.78 Option () is correct.

SOL 8.79 Option (B is correct.

If op-amp is ideal, no current will enter in op-amp. So current i_x is

$$i_x = \frac{v_x - v_y}{1\times 10^6} \qquad \ldots(1)$$

$$v_+ = v_- = v_x \qquad \text{(ideal op-amp)}$$

$$\frac{v_x - v_y}{100\times 10^3} + \frac{v_x - 0}{10\times 10^3} = 0$$

$$v_x - v_y + 10 v_x = 0$$

$$11 v_x = v_y \qquad \ldots(2)$$

For equation (1) & (2)

$$i_x = \frac{v_x - 11 v_x}{1\times 10^6} = -\frac{10 v_x}{10^6}$$

Input impedance of the circuit.

$$R_{in} = \frac{v_x}{i_x} = -\frac{10^6}{10} = -\,100\,\text{k}\Omega$$

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SOL 8.80 Option (A) is correct.

Given Boolean expression,

$$\begin{aligned} Y &= (\overline{A}\cdot BC + D)(\overline{A}\cdot D + \overline{B}\cdot \overline{C}) \\ &= (\overline{A}\cdot BCD) + (\overline{A}BC\cdot \overline{B}\cdot \overline{C}) + (\overline{A}D) + \overline{B}\,\overline{C}D \\ &= \overline{A}\,BCD + \overline{A}D + \overline{B}\,\overline{C}\,D \\ &= \overline{A}D(BC+1) + \overline{B}\,\overline{C}D = \overline{A}D + \overline{B}\,\overline{C}\,D \end{aligned}$$

SOL 8.81 Option (D) is correct.

In the given circuit, output is given as.

$$Y = (A_0 \oplus B_0) \odot (A_1 \oplus B_1) \odot (A_2 \oplus B_2) \odot (A_3 \oplus B_3)$$

For option (A)

$$\begin{aligned} Y &= (1 \oplus 1) \odot (0 \oplus 0) \odot (1 \oplus 1) \odot (0 \oplus 0) \\ &= 0 \odot 0 \odot 0 \odot 0 = 1 \end{aligned}$$

For option (B)

$$\begin{aligned} Y &= (0 \oplus 0) \odot (1 \oplus 1) \odot (0 \oplus 0) \odot (1 \oplus 1) \\ &= 0 \odot 0 \odot 0 \odot 0 = 1 \end{aligned}$$

For option (C)

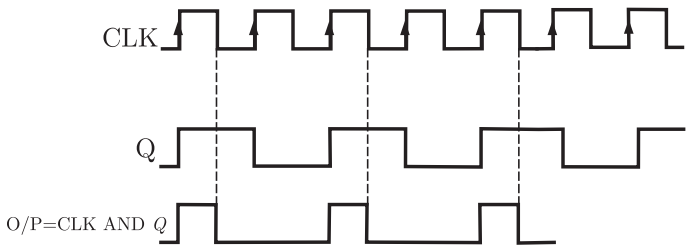
$$\begin{aligned} Y &= (0 \oplus 0) \odot (0 \oplus 0) \odot (1 \oplus 1) \odot (0 \oplus 0) \\ &= 0 \odot 0 \odot 0 \odot 0 = 1 \end{aligned}$$

For option (D)

$$\begin{aligned} Y &= (1 \oplus 1) \odot (0 \oplus 0) \odot (1 \oplus 1) \odot (0 \oplus 1) \\ &= 0 \odot 0 \odot 0 \odot 1 = 0 \end{aligned}$$

SOL 8.82 Option (B) is correct.

In the given circuit, waveforms are given as,



SOL 8.83 Option (C) is correct.

The program is executed in following steps.

START MVI A, 14H → one instruction cycle.

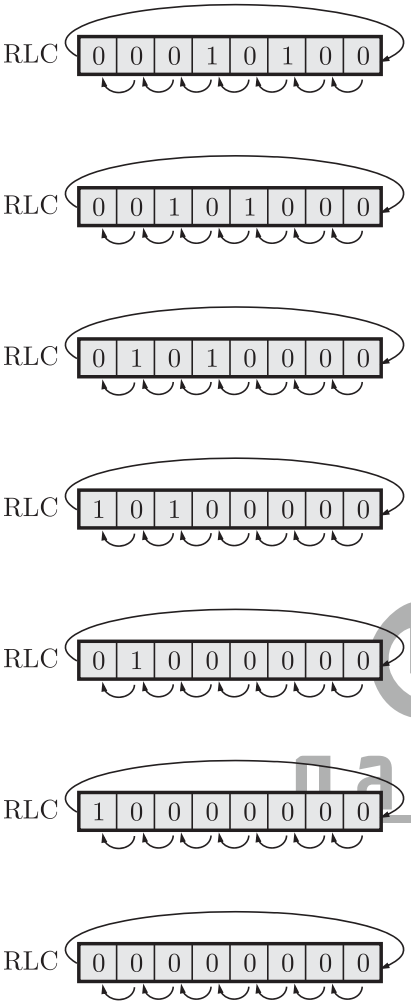
RLC ⇒ rotate accumulator left without carry

RLC is executed 6 times till value of accumulator becomes zero.

JNZ, JNZ checks whether accumulator value is zero or not, it is executed 5

times.

HALT → 1-instruction cycle.



So total no. of instruction cycles are

$$n = 1 + 6 + 5 + 1$$
$$= 13$$

SOL 8.84 Option (B) is correct.

In the given circuit

$$V_i = 0 \text{ V}$$

So, transistor Q_1 is in cut-off region and Q_2 is in saturation.

$$5 - I_C R_C - V_{CE(\text{sat})} - 1.25 = 0$$
$$5 - I_C R_C - 0.1 - 1.25 = 0$$
$$5 - I_C R_C = 1.35$$
$$V_0 = 1.35 \qquad \{\because V_0 = 5 - I_C R_C$$

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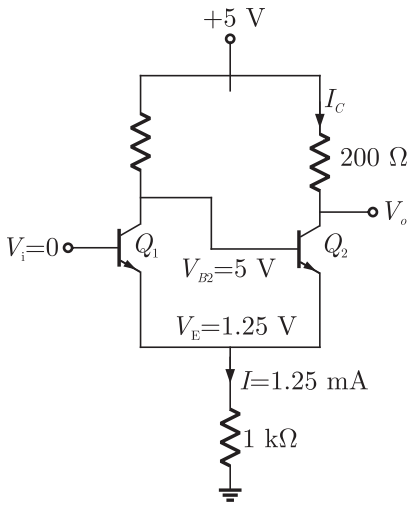

SOL 8.85 Option (C) is correct.

Since there exists a drain current for zero gate voltage ($V_{GS} = 0$), so it is a depletion mode device.

I_D increases for negative values of gate voltages so it is a p-type depletion mode device.

SOL 8.86 Option (B) is correct.

Applying KVL in input loop,

$$4 - (33 \times 10^3)\, I_B - V_{BE} - (3.3 \times 10^3)\, I_E = 0 \qquad \because I_E = (h_{fe} + 1)\, I_B$$

$$4 - (33 \times 10^3)\, I_B - 0.7 - (3.3 \times 10^3)\, (h_{fe} + 1)\, I_B = 0$$

$$3.3 = [(33 \times 10^3) + (3.3 \times 10^3)\,(99 + 1)]\, I_B$$

$$I_B = \frac{3.3}{33 \times 10^3 + 3.3 \times 10^3 \times 100}$$

$$I_C = h_{fe} I_B$$

$$= \frac{99 \times 3.3}{[0.33 + 3.3] \times 100} \text{ mA} = \frac{3.3}{0.33 + 3.3} \text{ mA}$$

SOL 8.87 Option (D) is correct.

Let the voltages at positive and negative terminals of op-amp are v_+ and v_- respectively. Then by applying nodal equations.

$$\frac{v_- - v_{in}}{R_1} + \frac{v_- - v_{out}}{R_1} = 0$$

$$2\, v_- = v_{in} + v_{out} \qquad ..(1)$$

Similarly,

$$\frac{v_+ - v_{in}}{R} + \frac{v_+ - 0}{\left(\frac{1}{j\omega C}\right)} = 0$$

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$$v_+ - v_{in} + v_+(j\omega CR) = 0$$
$$v_+(1 + j\omega CR) = V_{in} \quad ..(2)$$

By equation (1) & (2)

$$\frac{2v_{in}}{1 + j\omega CR} = v_{in} + v_{out} \qquad \{\because v_+ = v_- \text{ (ideal op-amp)}$$
$$v_{in}\left[\frac{2}{1 + j\omega CR} - 1\right] = v_{out}$$
$$v_{out} = v_{in}\frac{(1 - j\omega CR)}{1 + j\omega CR}$$

Phase shift in output is given by

$$\theta = \tan^{-1}(-\omega CR) - \tan^{-1}(\omega CR)$$
$$= \pi - \tan^{-1}(\omega CR) - \tan^{-1}(\omega CR)$$
$$= \pi - 2\tan^{-1}(\omega CR)$$

Maximum phase shift $\theta = \pi$

SOL 8.88 Option (C) is correct.

In given circuit MUX implements a 1-bit full adder, so output of MUX is given by.

$$F = \text{Sum} = \text{A} \oplus \text{Q} \oplus \text{C}_{in}$$

Truth table can be obtain as.

P	Q	C_{in}	Sum
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$\text{Sum} = \overline{P}\,\overline{Q}\,C_{in} + \overline{P}Q\,\overline{C_{in}} + P\,\overline{Q}\,\overline{C_{in}} + P\,Q\,C_{in}$$

Output of MUX can be written as

$$F = \overline{P}\,\overline{Q}\cdot I_0 + \overline{P}Q\cdot I_1 + P\overline{Q}\cdot I_2 + PQ\cdot I_3$$

Inputs are,

$$I_0 = C_{in},\quad I_1 = \overline{C_{in}},\quad I_2 = \overline{C_{in}},\quad I_3 = C_{in}$$

SOL 8.89 Option (D) is correct.

Program counter contains address of the instruction that is to be executed next.

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SOL 8.90 Option (A) is correct.

For a n-channel enhancement mode MOSFET transition point is given by,

$$V_{DS(\text{sat})} = V_{GS} - V_{TH} \qquad \because\ V_{TH} = 2 \text{ volt}$$

$$V_{DS(\text{sat})} = V_{GS} - 2$$

From the circuit,

$$V_{DS} = V_{GS}$$

So $$V_{DS(\text{sat})} = V_{DS} - 2 \ \Rightarrow V_{DS} = V_{DS(\text{sat})} + 2$$

$$V_{DS} > V_{DS(\text{sat})}$$

Therefore transistor is in saturation region and current equation is given by.

$$I_D = K(V_{GS} - V_{TH})^2$$

$$4 = K(V_{GS} - 2)^2$$

V_{GS} is given by

$$V_{GS} = V_{DS} = 10 - I_D R_D = 10 - 4 \times 1 = 6 \ \text{ Volt}$$

So,

$$4 = K(6-2)^2$$

$$K = \frac{1}{4}$$

Now R_D is increased to 4 kΩ, Let current is I_D' and voltages are $V_{DS}' = V_{GS}'$

Applying current equation.

$$I_D' = K(V_{GS}' - V_{TH})^2$$

$$I_D' = \frac{1}{4}(V_{GS}' - 2)^2$$

$$V_{GS}' = V_{DS}' = 10 - I_D' \times R_D' = 10 - 4I_D'$$

So,

$$4I_D' = (10 - 4I_D' - 2)^2 = (8 - 4I_D')^2$$

$$= 16(2 - I_D')^2$$

$$I_D' = 4(4 + I_D'^2 - 4I_D')$$

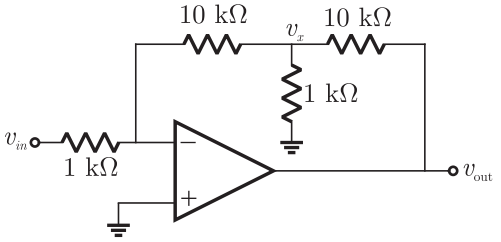
$$4I_D'^2 - 17 + 16 = 0$$

$$I_D'^2 = 2.84 \text{ mA}$$

SOL 8.91 Option (D) is correct.

Let the voltages at input terminals of op-amp are v_- and v_+ respectively.

So, $v_+ = v_- = 0$ (ideal op-amp)



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Applying node equation at negative terminal of op-amp,

$$\frac{0 - v_{in}}{1} + \frac{0 - v_x}{10} = 0 \qquad ...(1)$$

At node x

$$\frac{v_x - 0}{10} + \frac{v_x - v_{out}}{10} + \frac{v_x - 0}{1} = 0$$

$$v_x + v_x - v_{out} + 10v_x = 0$$

$$12\, v_x = v_{out}$$

$$v_x = \frac{v_{out}}{12}$$

From equation (1),

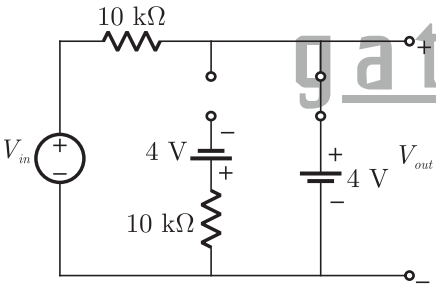
$$\frac{v_{in}}{1} + \frac{v_x}{10} = 0$$

$$v_{in} = -\frac{v_{out}}{120}$$

$$\frac{v_{out}}{v_{in}} = -120$$

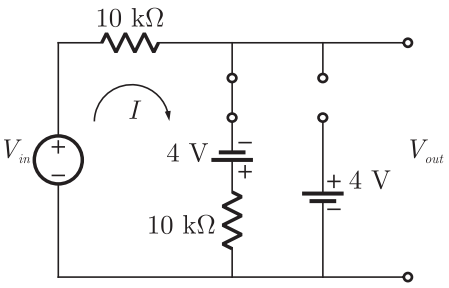
SOL 8.92 Option (D) is correct.

In the positive half cycle (when $V_{in} > 4$ V) diode D_2 conducts and D_1 will be off so the equivalent circuit is,



$$V_{out} = +4 \text{ Volt}$$

In the negative half cycle diode D_1 conducts and D_2 will be off so the circuit is,



Applying KVL

$$V_{in} - 10I + 4 - 10I = 0$$

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$$\frac{V_{in}+4}{20} = I$$

$V_{in} = -10$ V (Maximum value in negative half cycle)

So, $$I = \frac{-10+4}{20} = -\frac{3}{10} \text{ mA}$$

$$\frac{V_{in}-V_{out}}{10} = I$$

$$\frac{-10-V_{out}}{10} = -\frac{3}{10}$$

$$V_{out} = -(10-3)$$

$$V_{out} = -7 \text{ volt}$$

SOL 8.93 Option (C) is correct.

In the circuit, the capacitor charges through resistor $(R_A + R_B)$ and discharges through R_B. Charging and discharging time is given as.

$$T_C = 0.693(R_A + R_B)\text{C}$$

$$T_D = 0.693 R_B \text{C}$$

Frequency $$f = \frac{1}{T} = \frac{1}{T_D + T_C} = \frac{1}{0.693(R_A + 2R_B)C}$$

$$\frac{1}{0.693(R_A + 2R_B) \times 10 \times 10^{-9}} = 10 \times 10^3$$

$$14.4 \times 10^3 = R_A + 2R_B \quad \ldots(1)$$

$$\text{duty cycle} = \frac{T_C}{T} = 0.75$$

$$\frac{0.693(R_A + R_B)C}{0.693(R_A + 2R_B)C} = \frac{3}{4}$$

$$4R_A + 4R_B = 3R_A + 6R_B$$

$$R_A = 2R_B \quad \ldots(2)$$

From (1) and (2)

$$2R_A = 14.4 \times 10^3$$

$$R_A = 7.21 \text{ k}\Omega$$

and $$R_B = 3.60 \text{ k}\Omega$$

SOL 8.94 Option (B) is correct.

Given boolean expression can be written as,

$$F = \overline{X}Y\overline{Z} + \overline{X}\,\overline{Y}Z + X\overline{Y}Z + XY\overline{Z} + XYZ$$

$$= \overline{X}\,Y\overline{Z} + \overline{Y}Z(X + \overline{X}) + XY(\overline{Z} + Z)$$

$$= \overline{X}Y\overline{Z} + \overline{Y}Z + XY$$

$$= \overline{Y}Z + Y(X + \overline{X}\,\overline{Z}) \quad \because \; A + BC = (A + B)(A + C)$$

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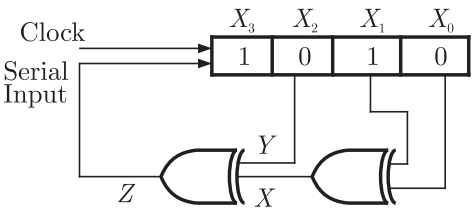
$$= \overline{Y}Z + Y(X + \overline{X})(X + \overline{Z})$$
$$= \overline{Y}Z + Y(X + \overline{Z})$$
$$= \overline{Y}Z + YX + Y\overline{Z}$$

SOL 8.95 Option (B) is correct.



$$X = X_1 \oplus X_0,\ Y = X_2$$

Serial Input $Z = X \oplus Y = [X_1 \oplus X_0] \oplus X_2$

Truth table for the circuit can be obtain as.

Clock pulse	Serial Input	Shift register
Initially	1	1010
1	0	1101
2	0	0110
3	0	0011
4	1	0001
5	0	1000
6	1	0100
7	1	1010

So after 7 clock pulses contents of the shift register is 1010 again.

SOL 8.96 Option (D) is correct.

Characteristic table of the X-Y flip flop is obtained as.

X	Y	Q_n	Q_{n+1}
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	0	0

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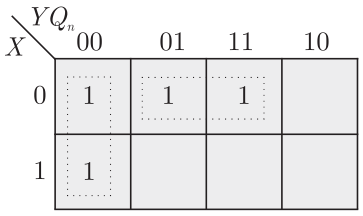
Solving from k-map



Characteristic equation of X-Y flip flop is

$$Q_{n+1} = \overline{Y}\,\overline{Q_n} + \overline{X}Q_n$$

Characteristic equation of a J-K flip-flop is given by

$$Q_{n+1} = \overline{K}Q_n + J\,\overline{Q_n}$$

by comparing above two characteristic equations

$$J = \overline{Y},\ K = X$$

SOL 8.97 Option (A) is correct.

Total size of the memory system is given by.

$$= (2^{12} \times 4) \times 8 \text{ bits}$$
$$= 2^{14} \times 8 \text{ bits}$$
$$= 2^{14} \text{ Bytes}$$
$$= 16\,\text{K bytes}$$

SOL 8.98 Option (C) is correct.

Executing all the instructions one by one.

$$\text{LXI H,1FFE} \Rightarrow \text{H} = (1\text{F})_{\text{H}},\ \ \text{L} = (\text{FE})_{\text{H}}$$
$$\text{MOV B,M} \Rightarrow \text{B} = \text{Memory [HL]} = \text{Memory [1FFE]}$$
$$\text{INR L} \Rightarrow \text{L} = \text{L} + (1)_{\text{H}} = (\text{FF})_{\text{H}}$$
$$\text{MOV A,M} \Rightarrow \text{A} = \text{Memory [HL]} = \text{Memory [1FFF]}$$
$$\text{ADD B} \Rightarrow \text{A} = \text{A} + \text{B}$$
$$\text{INR L} \Rightarrow \text{L} = \text{L} + (1)_{\text{H}} = (\text{FF})_{\text{H}} + (1)_{\text{H}} = 00$$
$$\text{MOV M,A} \Rightarrow \text{Memory [HL]} = \text{A}$$
$$\text{Memory [1F00]} = \text{A}$$
$$\text{XOR A} \Rightarrow \text{A} = \text{A XOR A} = 0$$

So the result of addition is stored at memory address 1F00.

SOL 8.99 Option (D) is correct.

Let the initial state Q(t) = 0, So $D = \overline{Q} = 1$, the output waveform is.

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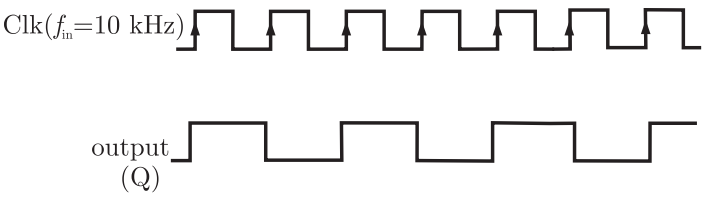


So frequency of the output is,

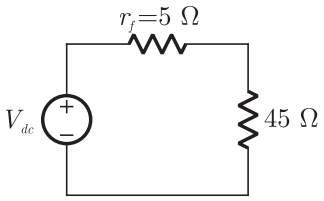
$$f_{out} = \frac{f_{in}}{2} = \frac{10}{2} = 5 \text{ kHz}$$

SOL 8.100 Option (A) is correct.

This is a half-wave rectifier circuit, so the DC voltage is given by

$$V_{dc} = \frac{V_m}{\pi}$$

Equivalent circuit with forward resistance is



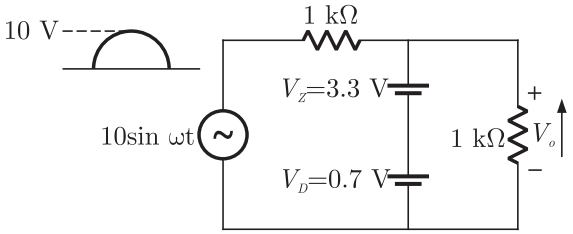
DC current in the circuit

$$I_{dc} = \frac{\frac{V_m}{\pi}}{r_f + R} = \frac{(V_m/\pi)}{(5+45)}$$

$$I_{dc} = \frac{V_m}{50\pi}$$

SOL 8.101 Option (B) is correct.

In the positive half cycle zener diode (D_z) will be in reverse bias (behaves as a constant voltage source) and diode (D) is in forward bias. So equivalent circuit for positive half cycle is.



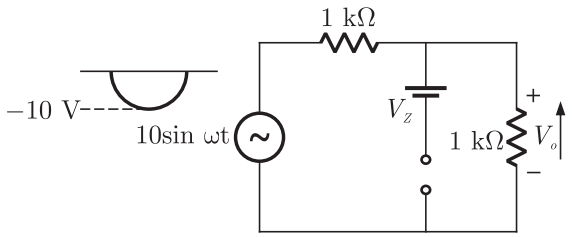
Output $V_o = V_D + V_z$

$= 0.7 + 3.3$

$= 4$ Volt

In the negative halt cycle, zener diode (D_z) is in forward bias and diode (D)

is in reverse bias mode. So equivalent circuit is.



So the peak output is,

$$V_o = \frac{10}{(1+1)} \times 1$$

$$V_o = 5 \text{ Volt}$$

SOL 8.102 Option (A) is correct.

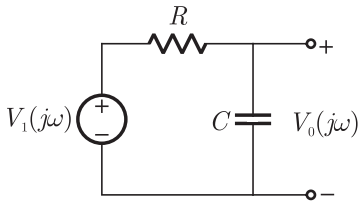
For active low chip select $\overline{CS} = 0$, so the address range can be obtain as,

$A_{15}A_{14}A_{13}A_{12}$	$A_{11}A_{10}A_9A_8$	$A_7A_6A_5A_4$	$A_3A_2A_1A_0$
1110	0000	0000	0000
⋮	⋮	⋮	⋮
1110	1111	1111	1111

So address range is E000-EFFF

SOL 8.103 Option (C) is correct.

A first order low pass filter is shown in following figure.



Transfer function

$$H(j\omega) = \frac{V_0(j\omega)}{V_i(j\omega)} = \frac{1}{R + \frac{1}{j\omega C}} \times \frac{1}{j\omega C} = \frac{1}{j\omega cR + 1}$$

Given that $|H(j\omega_1)| = 0.25$

$$\frac{1}{\sqrt{\omega_1^2 C^2 R^2 + 1}} = \frac{1}{4}$$

$$16 = \omega_1^2 R^2 C^2 + 1$$

$$\omega_1^2 R^2 C^2 = 15$$

$$4\pi^2 f_1^2 (50)^2 (5 \times 10^{-6})^2 = 15$$

$$f_1 = 2.46 \text{ kHz}$$

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SOL 8.104 Option (A) is correct.

In the circuit, voltage at positive terminal of op-amp is given by

$$\frac{v_+ - v_o}{10} + \frac{v_+ - 2}{3} = 0$$

$$3(v_+ - v_o) + 10(v_+ - 2) = 0$$

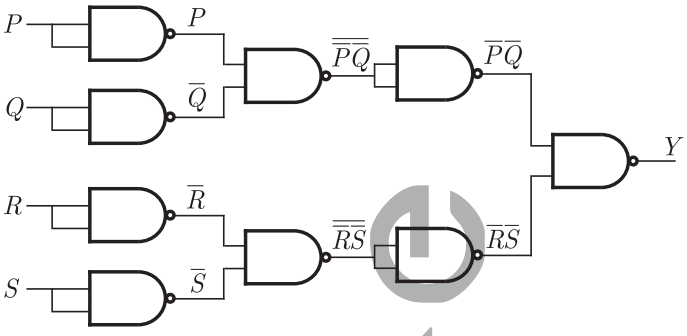
$$13v_+ = 20 + 3v_o$$

Output changes from $+15\,\text{V}$ to $-15\,\text{V}$,when $v_- > v_+$

$$v_+ = \frac{20 + (3 \times 15)}{13} = 5\,\text{Volt (for positive half cycle)}$$

SOL 8.105 Option (B) is correct.

Output for each stage can be obtain as,



So final output Y is.

$$Y = \overline{\overline{P}\,\overline{Q} \cdot \overline{R}\,\overline{S}} = \overline{(P+Q)} \cdot \overline{(R+S)} \qquad \because \overline{AB} = \overline{A} + \overline{B}$$

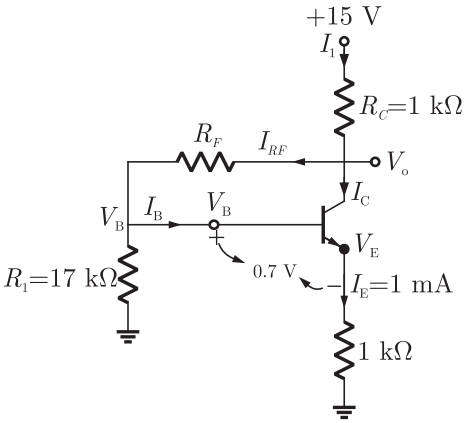
$$= P + Q + R + S$$

SOL 8.106 Option (B) is correct.

We can analyze that the transistor is in active region.

$$I_C = \frac{\beta}{(\beta+1)} I_E = \frac{99}{(99+1)}(1\text{ mA}) = 0.99\,\text{mA}$$

In the circuit



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In the circuit

$$V_{BE} = 0.7 \text{ V}$$

$$V_E = I_E \times 1 \text{ k}\Omega = 1 \text{ V}$$

$$V_B - V_E = 0.7$$

$$V_B = 0.7 + 1 = 1.7 \text{ volt}$$

Current through R_1

$$I_{R_1} = \frac{V_B}{17 \text{ k}\Omega} = \frac{1.7}{17 \text{ k}\Omega} = 100 \ \mu\text{A}$$

$$I_B = \frac{I_E}{\beta + 1} = \frac{1 \text{ mA}}{(99 + 1)} = 10 \ \mu\text{A}$$

Current through R_F , by writing KCL at Base

$$I_{RF} = I_B + I_{R1}$$

$$= 10 + 100 = 110 \ \mu\text{A}$$

Current through R_C

$$I_1 = I_C + I_{RF} = 0.99 \text{ mA} + 110 \ \mu\text{A} = 1.1 \text{ mA}$$

SOL 8.107 Option (D) is correct.

Output voltage

$$V_0 = 15 - I_1 R_C$$

$$= 15 - (1.1 \text{ mA})(1 \text{ k}\Omega) = 13.9 \text{ V}$$

SOL 8.108 Option (A) is correct.

Current in R_F

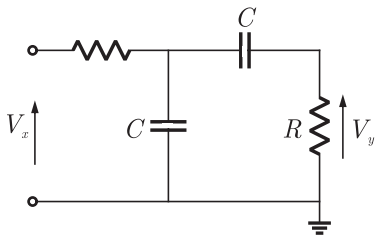
$$I_{RF} = \frac{V_0 - V_B}{R_F}$$

$$0.11 \text{ mA} = \frac{13.9 - 1.7 \text{ k}\Omega}{R_F}$$

$$R_F = 110.9 \text{ k}\Omega$$

SOL 8.109 Option (A) is correct.

By writing node equations in the circuit



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$$\frac{V_a - V_x}{R} + V_a Cs + (V_a - V_y) Cs = 0$$

or $$V_a(1 + 2RCs) - V_x - sCRV_y = 0 \quad ...(1)$$

or $$(V_y - V_a) Cs + \frac{V_y}{R} = 0$$

or $$V_y(1 + sCR) - V_a sCR = 0 \quad ...(2)$$

From equation (1) & (2)

$$\left(\frac{1 + sCR}{sCR}\right)(1 + 2sCR) V_y - V_x - sCRV_y = 0$$

$$V_y\left[\frac{(1 + sCR)(1 + 2sCR)}{sCR} - sCR\right] = V_x$$

$$V_y \frac{(1 + 3sCR + 2s^2C^2R^2 - s^2C^2R^2)}{sCR} = V_x$$

Transfer function

$$T(s) = \frac{V_y}{V_x} = \frac{sCR}{1 + 3sCR + s^2C^2R^2}$$

$$T(j\omega) = \frac{j\omega CR}{1 + j3\omega CR - C^2R^2\omega^2} = \frac{j\omega CR}{(1 - C^2R^2\omega^2) + 3j\omega CR}$$

SOL 8.110 Option (A) is correct.

Applying Barkhausen criterion of oscillation phase shift will be zero.

$$\angle T(j\omega_0) = 0 \qquad \omega_0 \rightarrow \text{frequency of oscillation.}$$

$$1 - C^2R^2\omega_0^2 = 0$$

$$\omega_0^2 = \frac{1}{R^2C^2}$$

$$\omega_0 = \frac{1}{RC}$$

SOL 8.111 Option (C) is correct.

In figure

$$V_y = \frac{V_0}{R_F + R} R$$

$$|T(j\omega)| = \frac{V_y}{V_0} = \left|\frac{j\omega_0 CR}{1 - \omega_0^2 C^2R^2 + j3\omega_0 CR}\right|$$

$$\omega = \frac{1}{RC}$$

So, $$\frac{V_y}{V_0} = \frac{j}{3j} = \frac{1}{3}$$

$$\frac{R}{R_F + R} = \frac{1}{3}$$

$$R_F = 2R = 2 \times 1 = 2\ \text{k}\Omega$$

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SOL 8.112 Option (C) is correct.

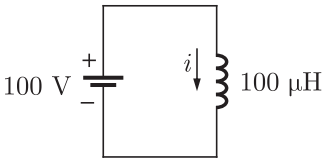
By writing truth table for the circuit

CLK	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
	1	0	1

All flip flops are reset. When it goes to state 101, output of NAND gate becomes 0 or $\overline{CLR} = 0$, so all FFs are reset. Thus it is modulo 4 counter.

SOL 8.113 Option (A) is correct.

When the switch is closed (i.e. during T_{ON}) the equivalent circuit is



Diode is off during T_{ON}.writing KVL in the circuit.

$$100 - (100 \times 10^{-6})\frac{di}{dt} = 0$$

$$\frac{di}{dt} = 10^6$$

$$i = \int 10^6\, dt = 10^6 t + i(0)$$

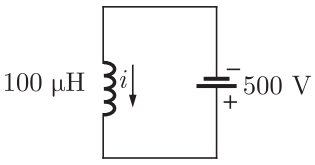
Since initial current is zero $i(0) = 0$

So, $$i = 10^6 t$$

After a duration of T_{ON} the current will be maximum given as

$$i_{Peak} = 10^6\ T_{ON}$$

When the switch is opened (i.e. during T_{off}) the equivalent circuit is



Diode is ON during T_{off}, writing KVL again

$$500 = -(100 \times 10^{-6})\frac{di}{dt}$$

$$i = -5 \times 10^6 t + i(0)$$

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$$i(0) = i_p = 10^6\, T_{ON}$$

So,

$$i = -5 \times 10^6 t + 10^6\ T_{ON}$$

After a duration of T_{off}, current $i = 0$

So, $$0 = -5 \times 10^6 t\, T_{off} + 10^6 T_{ON}$$

$\Rightarrow$ $$T_{ON} = 5\ T_{off}$$

Given that

$$T_{ON} + T_{off} = 100\ \mu sec$$

$$T_{ON} + \frac{T_{ON}}{5} = 100\ \mu sec$$

$$T_{ON} = \frac{100}{1.2} = 63.33\ \mu sec$$

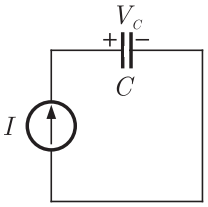
Peak current $$i_p = 10^6 \times T_{ON}$$

$$= 63.33 \times 10^{-6} \times 10^6 = 63.33\ A$$

SOL 8.114 Option (C) is correct.

When the switch is opened, current flows through capacitor and diode is ON in this condition.

so the equivalent circuit during T_{OFF} is



$$I = C\frac{dV_c}{dt}$$

$\Rightarrow$ $$V_c = \frac{I}{C}t + V_c(0)$$

Initially $$V_c(0) = 0$$

$$V_c = \frac{I}{C}t$$

At $$t = T_{off}$$

$$V_c = \frac{I}{C}T_{off}$$

Duty cycle $$D = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \frac{T_{ON}}{T}$$

$$T_{ON} = DT$$

$$T_{OFF} = T - T_{ON} = T - DT$$

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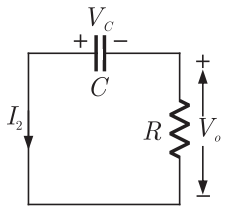
So, $$V_c = \frac{I}{C}(T - DT)$$

$$= \frac{I}{C}(1 - D)\, T$$

During T_{OFF}, output voltage $V_0 = 0$ volt.

SOL 8.115 Option (B) is correct.

When the switch is closed, diode is off and the circuit is



In steady state condition

$$C\,\frac{dV_c}{dt} = I_2$$

$$I_2 = C\frac{I}{C} \qquad \because \frac{dV_c}{dt} = \frac{I}{C}$$

$$V_0 = -\,V_c = \frac{-I}{C}t$$

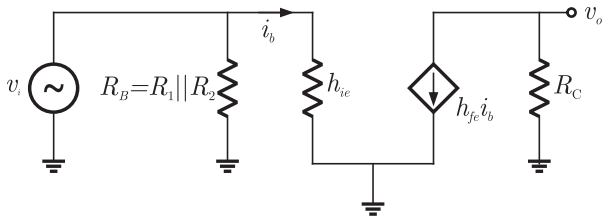
Average output voltage

$$V_0 = \frac{1}{T}\left[\int_0^{DT = T_{ON}} \left(-\frac{I}{C}t\right)dt + \int_0^{T_{OFF}} 0\, dt\right]$$

$$= -\frac{1}{T}\cdot\frac{I}{C}\left[\frac{t^2}{2}\right]_0^{DT} = -\frac{1}{T}\cdot\frac{I}{C}\cdot\frac{D^2T^2}{2} = -\frac{I}{C}\frac{D^2}{2}\cdot T$$

SOL 8.116 Option (B) is correct.

Equivalent hybrid circuit of given transistor amplifier when R_E is by passed is shown below.



In the circuit

$$i_b = \frac{v_s}{h_{ie}} \qquad \ldots(1)$$

$$v_o = h_{fe}\, i_b . R_C = h_{fe} . \frac{v_s}{h_{ie}} . R_C$$

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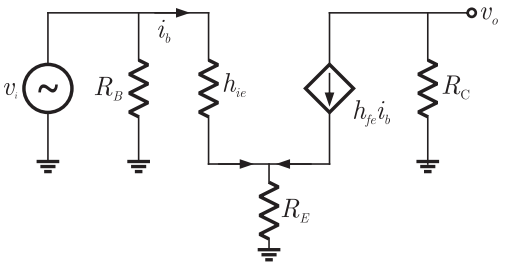
Voltage gain $A_{v_1} = \dfrac{v_o}{v_i} = \dfrac{h_{fe} R_C}{h_{ie}}$

Equivalent hybrid circuit when R_E is not bypassed by the capacitor.



In the circuit

$$v_s = i_b h_{ie} + (i_b + h_{fe} i_b) R_E$$

$$v_s = i_b [h_{ie} + (1 + h_{fe}) R_E] \quad ...(2)$$

$$v_0 = h_{fe} i_b . R_C \quad ...(3)$$

from equation (2) and (3)

$$v_0 = h_{fe} . R_C \frac{v_s}{h_{ie} + (1 + h_{fe}) R_E}$$

Voltage gain, $A v_2 = \dfrac{v_0}{v_s} = \dfrac{h_{fe} R_C}{h_{ie} + (1 + h_{fe}) R_E}$

So $\dfrac{A v_1}{A v_2} = \dfrac{h_{ie} + (1 + h_{fe}) R_E}{h_{ie}} = 1 + \dfrac{(1 + h_{fe}) R_E}{h_{ie}}$

$A_{v_2} < A_{v_1}$

SOL 8.117 Option (C) is correct.

Conversion time for different type of ADC is given as

Counting type $T_T \rightarrow$ Conversion time

$T_T = 2^n T_C$ $T_C \rightarrow$ Clock period

Integrating type

$$T_T = 2^{n+1} T_C$$

Successive Approximation type

$$T_T = n T_C$$

Parallel (flash) type $\rightarrow$ fastest

Conversion time is highest for integrating type ADC. So it is slowest.

SOL 8.118 Option (D) is correct.

$$F = \overline{A + B} \text{ (NOR)}$$

Output is 1 when $A = B = 0$

OR, $F = \text{A} \odot \text{B}$ (Ex-NOR)

Output is 1 when $A = B = 0$

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SOL 8.119 Option (B) is correct.

Output of the multiplexer is written as

$$f = I_0\overline{S_1}\,\overline{S_0} + I_1\overline{S_1}S_0 + I_2S_1\overline{S_0} + I_3S_1S_0$$

$$I_0 = 0,\ I_1 = I_2 = I_3 = 1$$

So,
$$f = 0 + \overline{x}y + x\overline{y} + xy = \overline{x}y + x\overline{y} + xy$$
$$= \overline{x}y + x(y + \overline{y}) = \overline{x}y + x \qquad \because y + \overline{y} = 1$$
$$= (\overline{x} + x)(x + y) \qquad A + BC = (A + B)(A + C)$$
$$= x + y \qquad \because \overline{x} + x = 1$$

SOL 8.120 Option (C) is correct.

Since gain-bandwidth product remains constant

Therefore $10^5 \times 10 = 100 \times f_{CL}$

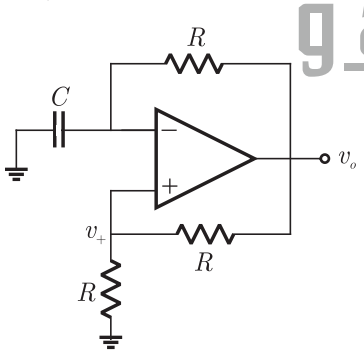
$$f_{CL} = 10 \text{ kHz}$$

SOL 8.121 Option (B) is correct.

Given circuit is an astable multi vibrator circuit, time period is given as

$$T = 2\tau \ln\left(\frac{1+\beta}{1-\beta}\right),\ \ \tau = RC$$

$\beta \rightarrow$ feedback factor



$$\beta = \frac{v_+}{v_o} = \frac{1}{2}$$

So,
$$T = 2\tau \ln\left(\frac{1+\frac{1}{2}}{1-\frac{1}{2}}\right) = 2\tau \ln 3$$

SOL 8.122 Option (C) is correct.

MVI A, 10 H $\Rightarrow$ MOV $(10)_H$ in accumulator

A $=(10)$H

MVI B, 10 H $\Rightarrow$ MOV $(10)_H$ in register B

B $= (10)_H$

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BACK : NOP

ADDB ⇒ Adds contents of register B to accumulator and result stores in accumulator

$$A = A + B = (10)_H + (10)_H$$

$$\begin{array}{r} 0\,0\,0\;\;1\,0\,0\,0\,0 \\ \underline{\text{ADD}\;\;0\,0\,0\;\;1\,0\,0\,0\,0} \\ A = 0\,0\,1\;\;0\,0\,0\,0\,0 \end{array}$$

$$= (20)_H$$

RLC ⇒ Rotate accumulator left without carry

acc | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | CY=0

RLC | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | $A=(40)_H$

JNC BACK ⇒ JUMP TO Back if $CY = 0$

NOP

ADD B ⇒ $A = A + B$

$$= (40)_H + (10)_H$$

$$\begin{array}{r} 0\,1\,0\,0\;\;0\,0\,0\,0 \\ \underline{\text{ADD}\;\;0\,0\,0\,1\;\;0\,0\,0\,0} \\ A = 0\,1\,0\,1\;\;0\,0\,0\,0 \end{array}$$

$$= (60)_H$$

| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | CY=0

RLC

A | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | CY=0

$$A = (A0)_H$$

JNC BACK

NOP

ADDB ⇒ $A = A + B$

$$= (A0)_H + (10)_H$$

$$\begin{array}{r} 1\,0\,1\,0\;\;0\,0\,0\,0 \\ \underline{\text{ADD}\;\;0\,0\,0\,1\;\;0\,0\,0\,0} \\ A = 1\,0\,1\,1\;\;0\,0\,0\,0 \end{array}$$

$$A = (B0)_H$$

| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | CY=0

RLC

A | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | CY=1

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CY = 1 So it goes to HLT.

therefore NOP will be executed 3 times.

SOL 8.123 Option (D) is correct.

Leakage current is given by

$$I_{\text{Leakage}} = \frac{Q'}{t} = \frac{0.5 \times \frac{1}{100} \times Q}{t} = \frac{0.5 \times \frac{1}{100} \times CV}{t}$$

$$= \frac{0.5 \times 10^{-2} \times 0.1 \times 10^{-9} \times 5}{1 \times 10^{-6}}$$

$$= \frac{25 \times 10^{-13}}{10^{-6}} = 2.5 \times 10^{-6} = 2.5\,\mu\text{A}$$

SOL 8.124 Option (A) is correct.

Slew rate is defined as the maximum rate of change in output voltage per unit time.

$$\text{Slew rate} = \frac{dv_0}{dt}$$

For voltage follower, $v_0 = v_{in}$

So, $$\text{Slew rate} = \frac{dv_{in}}{dt}, \quad v_{in} = 10\sin\omega t$$

$$= \frac{d}{dt}(10\sin\omega t) = 10\omega\cos\omega t$$

$$= 10\omega = 62.8 \text{ volt}/\mu\text{sec (given)}$$

$$10 \times 2\pi f = 62.8 \times 10^6$$

$$f = \frac{62.8 \times 10^6}{62.8} = 1 \text{ MHz}$$

SOL 8.125 Option (C) is correct.

Trans conductance of an n-channel JFET, is given by.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{-2I_{DSS}}{V_P}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Trans conductance (g_m) is maximum when gate - to - source voltage

$$V_{GS} = 0$$

$$(g_m)_{\max} = \frac{-2I_{DSS}}{V_P}$$

So, $$g_m = (g_m)_{\max}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Here $$1 = (g_m)_{\max}\left[1 - \frac{(-3)}{(-5)}\right] = (g_m)_{\max} \times \frac{2}{5}$$

$$(g_m)_{\max} = \frac{5}{2} = 2.5$$

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SOL 8.126 Option () is correct.

The circuit is a synchronous counter.

Where input to the flip flops are

$$D_3 = \overline{Q_3 + Q_2 + Q_1}$$

$$D_2 = Q_3,\ D_1 = Q_2,\ D_0 = Q_1$$

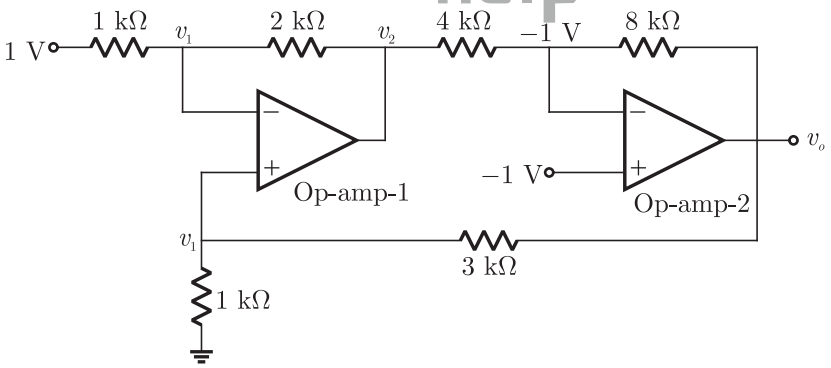
Truth table of the circuit can be drawn as

CLK	Q_3	Q_2	Q_1	Q_0
Initial state	1	1	1	0
1	0	1	1	1
2	0	0	1	1
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1
8	1	0	0	0

From the truth table we can see that counter states at $N = 4$ and $N = 8$ are same. So mod number is 4.

SOL 8.127 Option (B) is correct.

In the circuit



Writing node equation in the circuit at the negative terminal of op amp-1

$$\frac{v_1 - 1}{1} + \frac{v_1 - v_2}{2} = 0$$

$$3v_1 - v_2 = 2 \qquad \ldots(1)$$

Similarly, at the positive terminal of op amp-1

$$\frac{v_1 - v_o}{3} + \frac{v_1 - 0}{1} = 0$$

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$$4v_1 - v_o = 0 \qquad ...(2)$$

At the negative terminals of op-amp-2

$$\left(\frac{-1 - v_2}{4}\right) + \left(\frac{-1 - v_o}{8}\right) = 0$$

$$-2 - 2v_2 - 1 - v_o = 0$$

$$v_o + 2v_2 = -3 \qquad ...(3)$$

From equation (1) and (2)

$$3\frac{v_o}{4} - 2v_2 = 1$$

From equation (3)

$$\frac{3}{4}v_o - 2(-3 - v_o) = 1$$

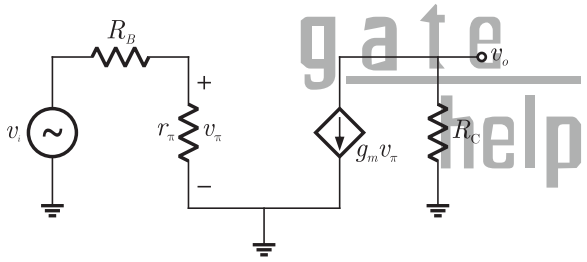
$$\frac{3}{4}v_o + v_o = -5$$

$$\frac{7}{4}v_o = -5$$

$$v_o = -\frac{20}{7} \text{ volt}$$

SOL 8.128 Option (C) is correct.

Small signal circuit is (mid-band frequency range)



$C_E \to 0$, for mid-band frequencies

$$v_o = -g_m v_\pi R_C$$

In the input loop

$$v_\pi = \frac{v_i r_\pi}{R_B + r_\pi}$$

So,
$$v_o = \frac{-g_m R_C r_\pi v_i}{R_B + r_\pi}$$

Gain
$$A_v = \frac{v_o}{v_i} = \frac{-g_m r_\pi R_C}{R_B + r_\pi}$$

Trans-conductance

$$g_m = \frac{I_C}{V_T} = \frac{(1 \text{ mA})}{(26 \text{ mV})} = \frac{1}{26} \text{ A/V}$$

$$g_m r_\pi = \beta_0 \Rightarrow r_\pi = \frac{\beta_0}{g_m} = 200 \times 26 = 5.2 \text{ k}\Omega$$

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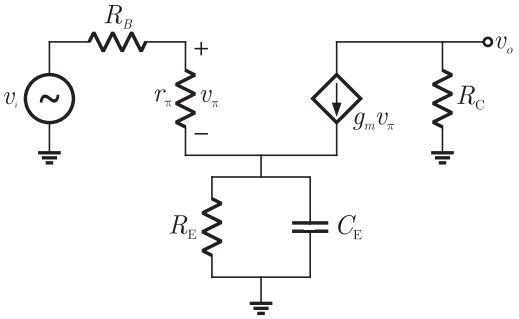
So gain $$A_v = \frac{-200 \times (1\ \text{k}\Omega)}{(25\ \text{k}\Omega + 5.2\ \text{k}\Omega)} = -6.62$$

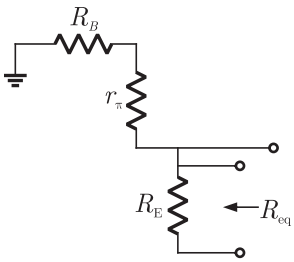
SOL 8.129 Option (B) is correct.

Cut off frequency due to C_E is obtained as



$$f_0 = \frac{1}{2\pi R_{eq} C_E}$$

Req → Equivalent resistance seen through capacitor C_E



$$\text{Req} = R_E \parallel R_B + r_\pi = \frac{R_E(R_B + r_\pi)}{R_E + R_B + r_\pi}$$

So $$f_0 = \frac{1(R_E + R_B + r_\pi)}{2\pi R_E (R_B + r_\pi) C_E} = 10\ \text{Hz (given)}$$

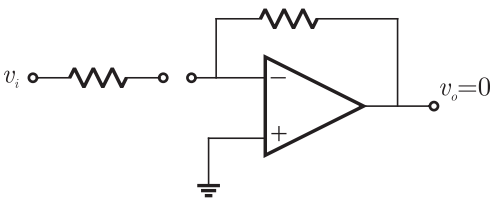
So, $$C_E = \frac{(0.1 + 25 + 5.2) \times 10^3}{2\pi \times 0.1\,(25 + 5.2) \times 10^6} = 1.59\ \text{mF}$$

SOL 8.130 Option (D) is correct.

We can approximately analyze the circuit at low and high frequencies as following.

For low frequencies $\omega \to 0 \Rightarrow \frac{1}{\omega_c} \to \infty$ (i.e. capacitor is open)

Equivalent circuit is



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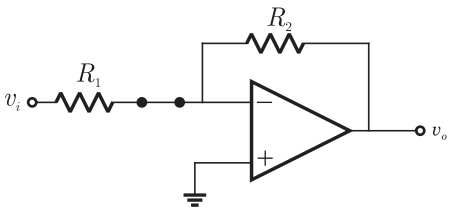
So, it does not pass the low frequencies.

For high frequencies $\omega \to \infty \Rightarrow \dfrac{1}{\omega_c} \to 0$ (i.e. capacitor is short)

Equivalent circuit is



$$v_o = -\frac{R_2}{R_1} v_i$$

So it does pass the high frequencies. This is a high pass filter.

SOL 8.131 At high frequency $\omega \to \infty \Rightarrow \dfrac{1}{\omega_c} \to 0$, capacitor behaves as short circuit and gain of the filter is given as

$$|A_v| = \left|-\frac{R_2}{R_1}\right| = 10$$

$$R_2 = 10\ R_1$$

Input resistance of the circuit $R_{in} = R_1 = 100\ \text{k}\Omega$

So, $R_2 = 10 \times 100\ \text{k}\Omega = 1\ \text{M}\Omega$

Transfer function of the circuit

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\omega R_2 C}{1 + j\omega R_1 C}$$

High frequency gain $|A_{v\infty}| = 10$

At cutoff frequency gain is

$$|A_v| = \frac{10}{\sqrt{2}} = \left|\frac{-j\omega_c R_2 C}{1 + j\omega_c R_1 C}\right|$$

$$\frac{10}{\sqrt{2}} = \frac{\omega_c R_2 C}{\sqrt{1 + \omega_c^2 R_1^2 C^2}}$$

$$100 + 100\omega_c^2 R_1^2 C^2 = 2\omega_c^2 R_2^2 C^2$$

$$100 + 100 \times \omega_c^2 \times 10^{10} \times C^2 = 2 \times \omega_c^2 \times 10^{12} \times C^2$$

$$100 = \omega_c^2 C^2 \times 10^{12}$$

$$C^2 = \frac{100}{\omega_c^2 \times 10^{12}}$$

$$C = \frac{1}{2\pi f_c \times 10^4} = \frac{1}{2 \times 3.14 \times 10^3 \times 10^4}$$

$$= 15.92\ \text{nF}$$

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